Xtium-CL MX4™

User's Manual

Edition 1.30

sensors | cameras | **frame grabbers** | processors | software | vision solutions

P/N: OC-Y4CM-MUSR0

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NOTICE

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About Teledyne DALSA

Teledyne DALSA is an international high performance semiconductor and electronics company that designs, develops, manufactures, and markets digital imaging products and solutions, in addition to providing wafer foundry services.

Teledyne DALSA Digital Imaging offers the widest range of machine vision components in the world. From industry-leading image sensors through powerful and sophisticated cameras, frame grabbers, vision processors and software to easy-to-use vision appliances and custom vision modules.

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Overview

Product Part Numbers

Xtium-CL MX4 Board

Item	Product Number
Xtium-CL MX4	OR-Y4C0-XMX00
For OEM clients, this manual in printed form, is available on request.	OC-Y4CM-MUSR0

Xtium-CL MX4 Software

Item	Product Number
Sapera LT version 8.20 or later for full feature support (required but sold separately). 1. Sapera LT: Provides everything needed to build imaging application. 2. Current Sapera-compliant board hardware drivers 3. Sapera documentation (compiled HTML help, Adobe Acrobat® (PDF)	OC-SL00-0000000
(optional) Sapera Processing Imaging Development Library includes over 600 optimized image-processing routines.	Contact Sales at Teledyne DALSA

Optional Xtium-CL MX4 Cables & Accessories

Item	Product Number
DH60-27S cable assembly to blunt end: 6 ft cable I/O 27 pin Hirose connector to blunt end. This cable assembly connects to J1. (see "J1: External Signals Connector (Female DH60-27P))	OR-YXCC-27BE2M1, Rev B1
Cable set to connect to J4 Internal I/O Signals connector (J4: 26-pin SHF-113-01-L-D-RA)	See suggested cables
DH40-27S Connector Kit for Custom Wiring: Comprised of a DH40-27S connector plus screw lock housing kit	OR-YXCC-H270000
Cable assembly to connect to J5 (Board Sync) Connecting 2 boards Connection 3 or 4 boards	 OR-YXCC-BSYNC20 OR-YXCC-BSYNC40
Power interface cable required when supplying power to cameras and/or J1/J4	OR-YXCC-PWRY00
Power Over Camera Link (PoCL) Video Input Cable 2 meter HDR to MDR 2 meter HDR to HDR	 OR-COMC-POCLD2 OR-COMC-POCLDH

About the Xtium-CL MX4 Frame Grabber

Series Key Features

- Compliant with Camera Link specification version 2.0
- Uses a PCIe x4 Gen2 slot to maximize transfers to host computer buffers
- Acquire from Monochrome, RGB, Bayer and Bi-Color cameras, both area scan and line scan
- Supports multiple tap formats, in multiple pixels depths
- Pixel clock range from 20 to 85 MHz
- Output lookup tables
- White Balance Gain for RGB pixels
- Vertical and Horizontal Flip supported on board
- Flat Field and Flat Line correction: pixel replacement using either neighborhood pixels or 3x2 cluster replacement.
- External Input Triggers and Shaft Encoder inputs, along with Strobe outputs
- Supports a number of acquisition events in compliance with "Trigger to Image Reliability"
- RoHS compliant
- Supports Power Over Camera Link (PoCL)

Supported Camera Link Configurations

The Camera Link industry standard is maintained by the Automated Imaging Association (AIA).

Camera Link configurations are Base, Medium, Full and Deca (Extended-Full).

Configuration	Data Bits	Maximum Throughput	Cables
Base	24	255 MB/s	1
Medium	48	510 MB/s	2
Full	64	680 MB/s	2
Deca (80-bits)	80	850 MB/s	2

User Programmable Configurations

The Xtium-CL MX4 supports the following Camera Link configurations, using one of 3 available firmware designs:

Firmware	Supported Camera Link Configurations
One Full Camera Link Input (*installation default selection*)	• 1 Base, 1 Medium or 1 Full Camera Link monochrome or bayer camera, 1/2/3/4/8 tap segmented, 2 taps alternate, or 2/3/4/8 taps parallel. • 1 Base or 1 Medium Camera Link RGB camera, 1 tap and 2 taps segmented/parallel. • Full Camera Link packed RGB camera.
One 80-bit Camera Link Input	• One 10 Tap @ 8-bit monochrome or bayer camera • One 8 Tap @ 10-bit monochrome or bayer camera • One 80-bit packed RGB camera • One 80-bit packed Bi-Color camera
Two Base Camera Link Input (any 2 of the supported configuration)	• Base Camera Link monochrome or Bayer camera, 1/2/3 tap segmented, 2 taps alternate, 2/3 taps parallel. • Base Camera Link RGB camera, 1 tap64

Use the Xtium-CL MX4 firmware firmware loader function in the Teledyne DALSA Device manager utility to select firmware for one of the supported modes. Firmware selection is made either during driver installation or manually later on (see Firmware Update: Manual Mode).

ACUPlus: Acquisition Control Unit

ACUPlus consists of a grab controller, one pixel packer, and one time base generator per camera input. ACUPlus delivers a flexible acquisition front end and supports pixel clock rates of up to 85MHz.

ACUPlus acquires variable frame sizes up to 64KB per horizontal line and up to 16 million lines per frame. ACUPlus can also capture an infinite number of lines from a line scan camera without losing a single line of data.

DTE: Intelligent Data Transfer Engine

The Xtium-CL MX4 intelligent Data Transfer Engine ensures fast image data transfers between the board and the host computer with zero CPU usage. The DTE provides a high degree of data integrity during continuous image acquisition in a non-real time operating system like Windows. DTE consists of multiple independent DMA units, Tap Descriptor Tables, and Auto-loading Scatter-Gather tables.

PCI Express x4 Gen2 Interface

The Xtium-CL MX4 is a universal PCI Express x4 Gen2 board, compliant with the PCI Express 2.0 specification. The Xtium-CL MX4 board achieves transfer rates up to 1.7 Gbytes/sec. to host memory. Note that performance can be lower depending on PC and/or programmed configuration.

The Xtium-CL MX4 board occupies one PCI Express x4 Gen2 expansion slot and one chassis opening.

Important:

- To obtain maximum transfer rate to host memory, make sure the Xtium-CL MX4 is in a Gen2 slot. Although the board will work in a Gen1 slot, only half the performance is achieved.
- The system motherboard BIOS should allow setting the PCIe maximum payload size to 256 MB or higher. Systems with fixed settings of 128 MB will limit performance for transfers to host memory.
- If the computer only has a PCI Express x16 slot, test directly or review the computer documentation to verify if the Xtium-CL MX4 is supported since computer motherboards may only support x16 graphic video board products in x16 slots.

Advanced Controls Overview

Visual Indicators

Xtium-CL MX4 features 3 LED indicators to facilitate system installation and setup. These indicators provide visual feedback on the board status and camera status.

External Event Synchronization

Trigger inputs and strobe signals precisely synchronize image captures with external events.

Camera Link Communications Ports

One PC independent communication port per camera input provides Camera Link camera configuration. This port does not require addition PC resources like free interrupts or I/O address space. Accessible via the board device driver, the communication port presents a seamless interface to Windows-based standard communication applications like HyperTerminal, etc. The communication port is accessible directly from the Camera Link connectors.

Quadrature Shaft Encoder

An important feature for web scanning applications, the Quadrature Shaft Encoder inputs allow synchronized line captures from external web encoders. The Xtium-CL MX4 provides an RS-422 or TTL (board revision B only, and mutually exclusive) input that supports a tick rate of up to 5 MHz.

Development Software Overview

Sapera++ LT Library

Sapera++ LT is a powerful development library for image acquisition and control. Sapera++ LT provides a single API across all current and future Teledyne DALSA hardware. Sapera++ LT delivers a comprehensive feature set including program portability, versatile camera controls, flexible display functionality and management, plus easy to use application development wizards. Applications are developed using either C++ or .NET frameworks.

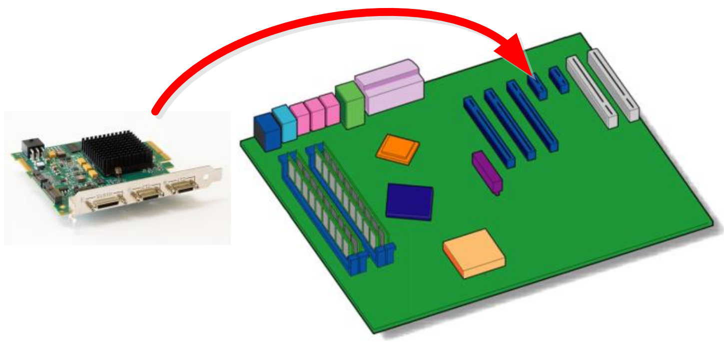
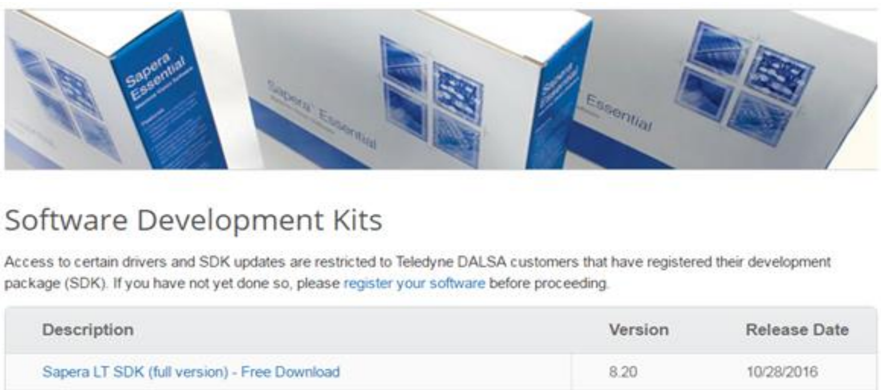
Sapera++ LT comes bundled with CamExpert, an easy to use camera configuration utility to create new, or modify existing camera configuration files.

Sapera Processing Library

Sapera Processing is a comprehensive set of C++ classes or .NET classes for image processing and analysis. Sapera Processing offers highly optimized tools for image processing, blob analysis, search (pattern recognition), OCR and barcode decoding.

Quick Start Setup & Installation

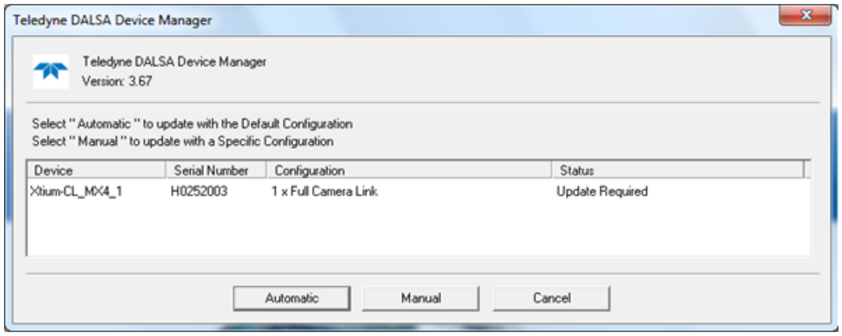
The following procedure outlines the basic steps required to install the Teledyne DALSA Xtium-CL MX4. For complete installation details and information, see Installing Xtium-CL MX4.

<table>
<tr><td>1</td><td>Install the Xtium-CL MX4 in an available PCIe x4 (or x8) slot on the host computer.

If using PoCL, connect power to the board J7 connector.</td></tr>
<tr><td>2</td><td>Download and install the Sapera LT SDK software from the Teledyne DALSA website.
http://teledynedalsa.com/imaging/support/downloads/sdks/

</td></tr>
<tr><td>3</td><td>Download and install the Xtium-CL MX4 device driver from the Teledyne DALSA website.
https://www.teledynedalsa.com/imaging/support/downloads/drivers/

</td></tr>
</table>

4

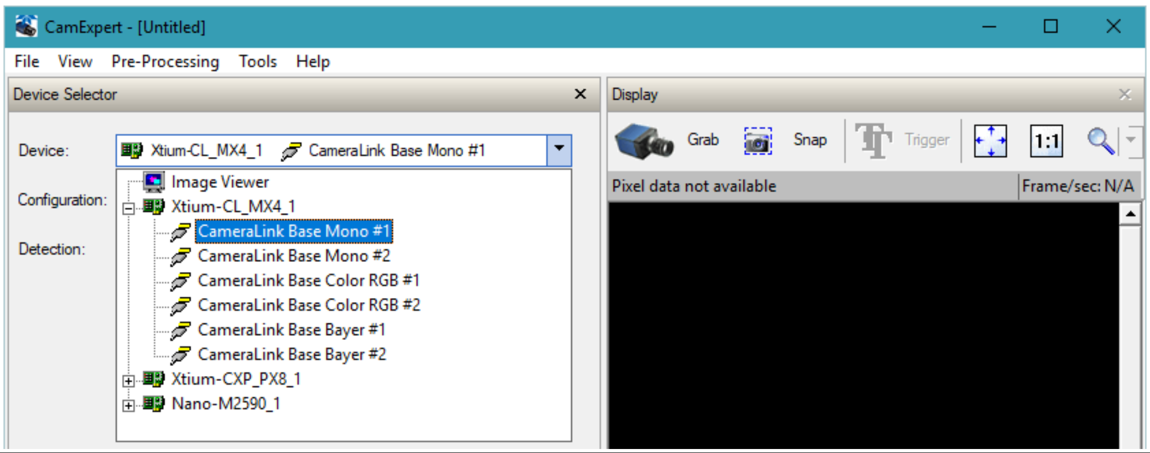
To complete the installation, update the Xtium-CL MX4 firmware when prompted; select Automatic to update with the default configuration (Full Camera Link) or Manual to select another option (2 Base Camera Link or 80-Bits Camera Link).



Reboot when all software and board drivers are installed.

5

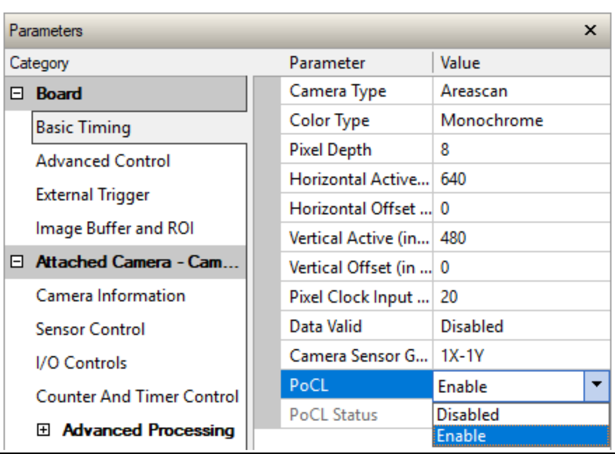
Launch Sapera LT CamExpert to verify the installation; the board should be present in the list of available devices.



6

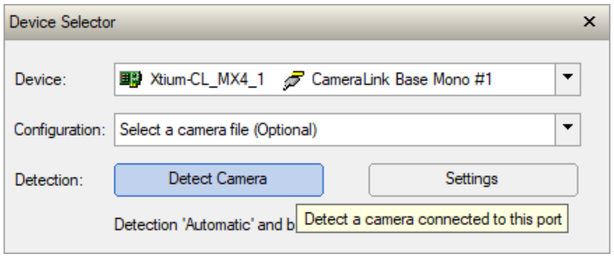
Connect camera(s) to the board Camera Link connectors. Ensure cameras are properly powered.

If using PoCL, use CamExpert to enable the PoCL feature in the the Basic Timing category.

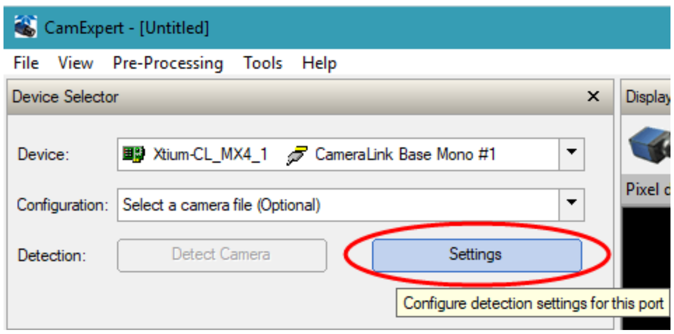


7

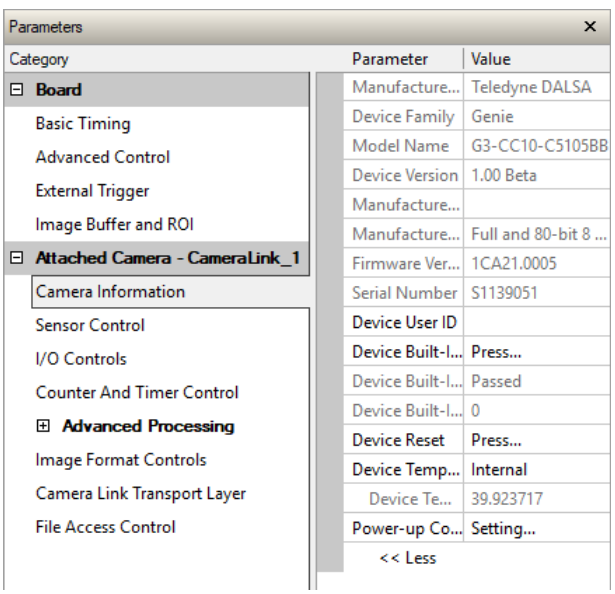
In CamExpert, click Detect Camera.



If the Detect Camera button is disabled, click Settings to open the the Communication Settings dialog to [configure CamExpert to detect attached cameras using a serial port](#).

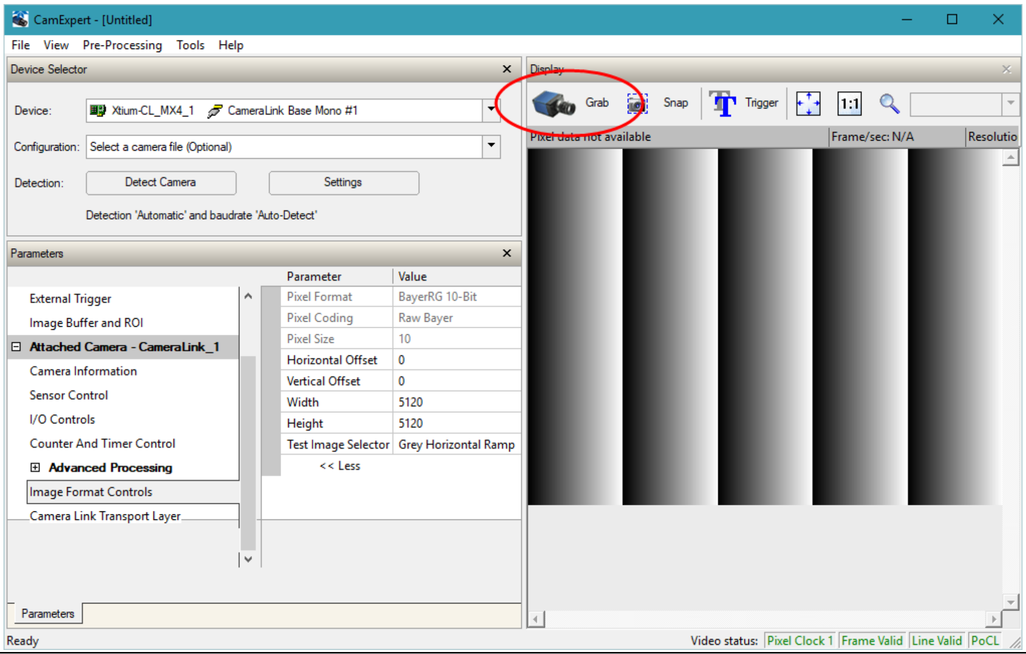


When CamExpert detects a camera (if GenCP compliant), camera parameters are displayed along with the board parameters.

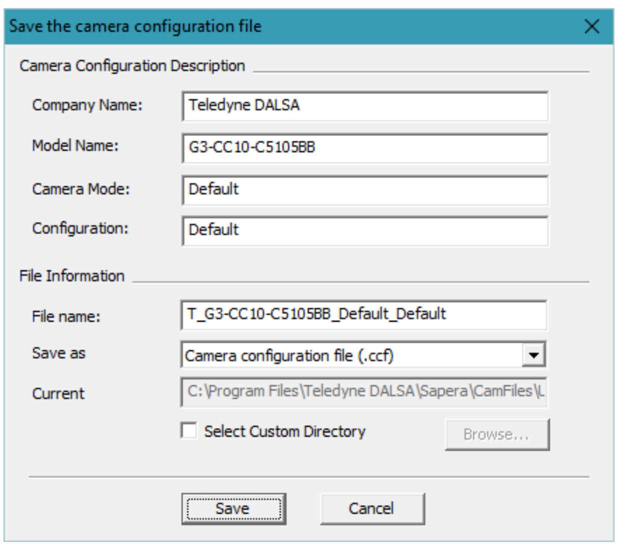


When properly connected, the video status bar displays camera signals in green.

8 Click Grab to acquire a test image to validate the setup.



9 Modify the board and camera parameters as necessary. When completed, save the [camera configuration file](#).



The Xtium-CL MX4 can be configured using the the parameter settings in this file when using the Sapera LT API in your application to acquire images

Installing Xtium-CL MX4

Warning! (Grounding Instructions)

Static electricity can damage electronic components. Please discharge any static electrical charge by touching a grounded surface, such as the metal computer chassis, before performing any hardware installation. If you do not feel comfortable performing the installation, please consult a qualified computer technician.

Important: Never remove or install any hardware component with the computer power on. Disconnect the power cord from the computer to disable the power standby mode. This prevents the case where some computers unexpectedly power up when a board is installed.

Installation

The Sapera LT Development Library (or 'runtime library' if application execution without development is preferred) must be installed before the Xtium-CL MX4 device driver.

The installation sequence is as follows:

- Turn the computer off, disconnect the power cord (disables power standby mode), and open the computer chassis to allow access to the expansion slot area.
- Install the Xtium-CL MX4 into a free PCI Express x4 Gen2 expansion slot (or an available x8 slot). Note that some computer's x16 slot may support the Xtium-CL MX4.
- Connect a spare power supply connector to J7 for PoCL cameras or when DC power is required on the external signals connector J1 or J4. See Power Cable Assembly OR-YXCC-PWRY00 for information about an adapter for older computers.
- Close the computer chassis and turn the computer on.
- Logon to the computer as administrator or with an account that has administrator privileges.

For information on performing a silent installation, refer to Appendix A: Silent Installation.

For troubleshooting installation problems, refer to Appendix B: Troubleshooting Installation Problems

Sapera LT Library & Xtium-CL MX4 Driver Installation

Sapera LT SDK (full version), the image acquisition and control SDK for Teledyne DALSA cameras and frame grabbers is available for download from the Teledyne DALSA website:

http://teledynedalsa.com/imaging/support/downloads/sdks/

Run-time versions are also available for download at this location.

Software Development Kits

Access to certain drivers and SDK updates are restricted to Teledyne DALSA customers that have registered their development package (SDK). If you have not yet done so, please register your software before proceeding.

Description	Version	Release Date
Sapera LT SDK (full version) - Free Download	8.30	05/19/2017

> The Sapera LT SDK installation includes compiled demo and example programs, along with project source code, in both C++ and .NET languages, for most Microsoft Visual Studio development platforms. The Sapera LT ++ and Sapera LT .NET demo source code are found in the Sapera\Demos directory.

Refer to *Sapera LT User's Manual* for additional details about Sapera LT.

Teledyne DALSA Device Drivers

All Teledyne DALSA device drivers are available for download from the Teledyne DALSA website:

https://www.teledynedalsa.com/imaging/support/downloads/drivers/

Installation Procedure

- Sapera LT is installed before Teledyne DALSA board drivers.
- Download the Sapera LT SDK from the Teledyne DALSA website and run the executable file; the installation menu is presented.
- The installation program may prompt to reboot the computer. It is not necessary to reboot the computer between the installation of Sapera LT and the board driver.
- Download the Xtium-CL MX4 device driver from the Teledyne DALSA website and run the executable file; the installation menu is presented.
- During the late stages of the installation, the Xtium-CL MX4 firmware loader application starts. This is described in detail in the following section.
- Reboot when all software and board drivers are installed.

> If Windows displays any unexpected message concerning the board, power off the system and verify the Xtium-CL MX4 is installed in the slot properly. You should also note the board's status LED color and compare it to the defined LED states as described in D1: Boot-up/PCIe Status LED.

Xtium-CL MX4 Firmware Loader

The Device Manager-Firmware Loader program automatically executes at the end of the driver installation and on every subsequent reboot of the computer. It will determine if the Xtium-CL MX4 requires a firmware update. If firmware is required, a dialog displays. This dialog also allows the user to load firmware for alternate operational modes of the Xtium-CL MX4.

	Important: In the rare case of firmware loader errors please see Recovering from a Firmware Update Error.

Firmware Update: Automatic Mode

Click **Automatic** to update the Xtium-CL MX4 firmware. The **Xtium-CL MX4** supports various firmware configurations with the default being a Full, Medium, or Base camera.

for details on all supported modes, selected via a manual firmware update.

With multiple Xtium-CL MX4 boards in the system, all are updated with new firmware. If any installed Xtium-CL MX4 board installed in a system already has the correct firmware version, an update is not required. In the following screen shot, a single Xtium-CL MX4 Full board is installed and ready for a firmware upgrade.

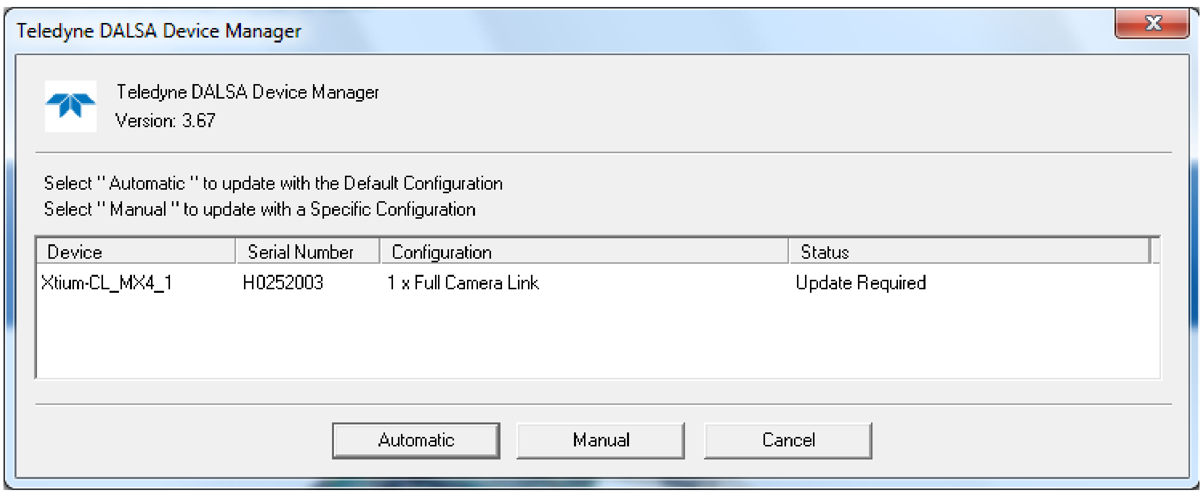


Figure 1: Automatic Firmware Update

Firmware Update: Manual Mode

Select **Manual** mode to load firmware other then the default version or when, in the case of multiple Xtium-CL MX4 boards in the same system, if each requires different firmware.

The following figure shows the Device Manager manual firmware screen. Displayed is information on all installed Xtium-CL MX4 boards, their serial numbers, and their firmware components.

Performing a Manual Firmware Update

To perform a manual firmware update:

- Select the Xtium-CL MX4 to update via the board selection box (if there are multiple boards in the system)
- From the Configuration field drop menu select the firmware version required (typical required to support different cameras)
- Click on the Start Update button

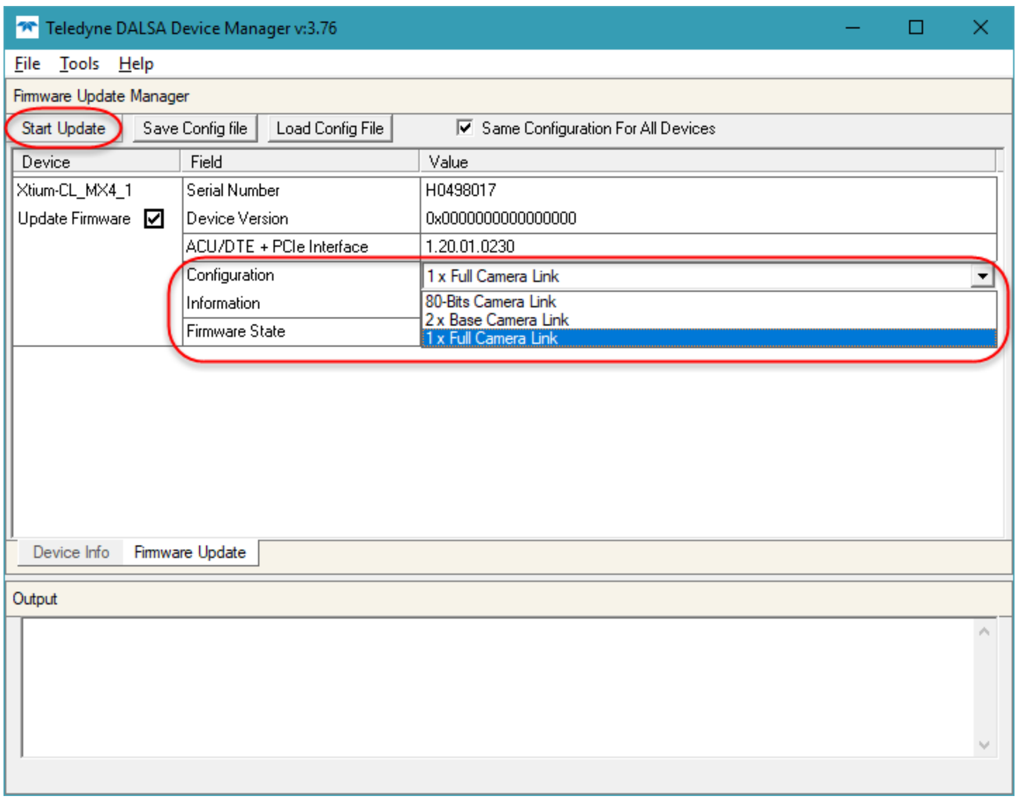


Figure 2: Manual Firmware Update

- Observe the firmware update progress in the message output window

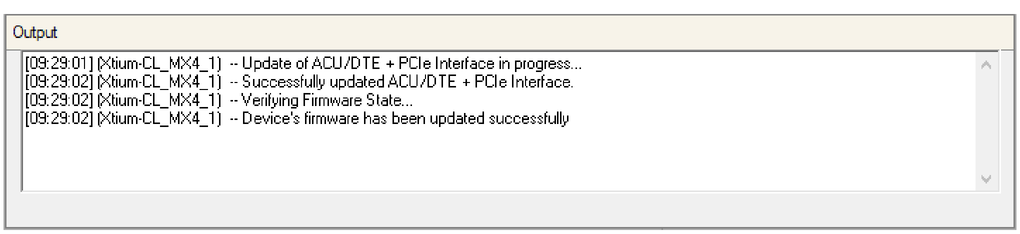


Figure 3: Firmware Update Progress

- Close the Device manager program when the device reset complete message is shown

Executing the Firmware Loader from the Start Menu

If required, the Xtium-CL MX4 Firmware Loader program is executed via the Windows Start Menu shortcut **Start • Programs • Teledyne DALSA • Xtium-CL MX4 Driver • Firmware Update**.

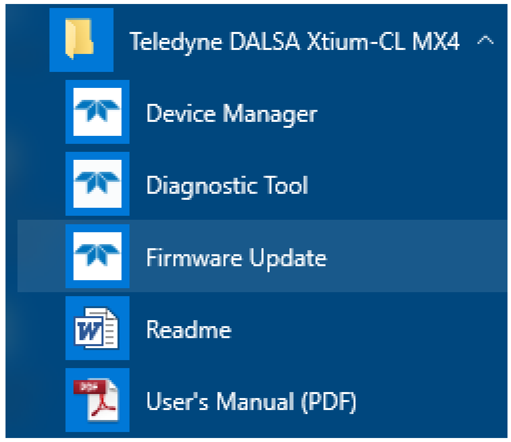


Figure 4: Start Menu Firmware Update Shortcut

A firmware change after installation is required to select a different configuration mode. For supported configurations, see the Supported Camera Link Configurations section.

Upgrading Sapera or Board Driver

When installing a new version of Sapera or a Teledyne DALSA acquisition board driver in a computer with a previous installation, the current version **must** be un-installed first. Described below are two upgrade situations. Note that if the board is installed in a different slot, the new hardware wizard opens. Answer as instructed in section Installation.

Board Driver Upgrade Only

Minor upgrades to acquisition board drivers are distributed as ZIP files available in the Teledyne DALSA web site www.teledynedalsa.com/mv/support. Board driver revisions are also available on the next release of the Sapera Essential CD-ROM.

Often minor board driver upgrades do not require a new revision of Sapera. To confirm that the current Sapera version will work with the new board driver:

- Check the new board driver ReadMe file before installing, for information on the minimum Sapera version required.
- If the ReadMe file does not specify the Sapera version required, contact Teledyne DALSA Technical Support (see Technical Support).

To upgrade the board driver only:

- Logon the computer as an administrator or with an account that has administrator privileges.
- In **Windows 7**, from the start menu select **Start • Settings • Control Panel • Programs and Features**. Double-click the Teledyne DALSA Xtium board driver and click **Remove**.
- In **Windows 8 & Windows 10**, just type Control Panel while in the start screen, or click the arrow in the lower left side to bring up the all applications window. Select Programs and Features, then double-click the Teledyne DALSA Xtium board driver and click **Remove**.
- Install the new board driver. Run **Setup.exe** if installing manually from a downloaded driver file.

	Important: You cannot install a Teledyne DALSA board driver without Sapera LT installed on the computer.

Upgrading both Sapera and Board Driver

When upgrading both Sapera and the acquisition board driver, follow the procedure described below.

- Logon the computer as an administrator or with an account that has administrator privileges.
- In **Windows 7**, from the start menu select **Start • Settings • Control Panel • Programs and Features**. Double-click the Teledyne DALSA Xtium board driver and click **Remove**. Follow by also removing the older version of Sapera LT.
- In **Windows 8 & Windows 10**, just type Control Panel while in the start screen, or click the arrow in the lower left side to bring up the all applications window. Select **Programs and Features**, then double-click the Teledyne DALSA Xtium board driver and click **Remove**. Do the same procedure with SaperaLT.
- Reboot the computer and logon the computer as an administrator again.
- Install the new versions of Sapera and the board driver as if this was a first time installation. See Sapera LT Library & Xtium-CL MX4 Driver Installation for installation procedures.

Using the Camera Link Serial Control Port

The Camera Link cabling specification includes a serial communication port for direct camera control by the frame grabber (see J3: Camera Link Connector 1). The Xtium-CL MX4 driver supports this serial communication port either directly (such as the Serial Command window in CamExpert) or by mapping it to a host computer COM port. Any serial port communication program, such as Windows HyperTerminal, can connect to the camera in use and modify its function modes via its serial port controls. The Xtium-CL MX4 serial port supports communication speeds from 9600 to 921600bps. The serial port is created by the kernel driver, so it will be available even if no Sapera LT application has started.

Note: if the serial communication program can directly select the Xtium-CL MX4 serial port then mapping to a system COM port is not necessary.

When required, map the Xtium-CL MX4 serial port to an available COM port by using the Sapera Configuration tool. Run the program from the Windows start menu: **Start • Programs • DALSA • Sapera LT • Sapera Configuration**.

COM Port Assignment

The lower section of the Sapera Configuration program screen contains the serial port configuration menu. Configure as follows:

- Use the **Physical Port** drop menu to select the Sapera board device from all available Sapera boards with serial ports (when more then one board is in the system).
- Use the **Optional COM Ports Mapping** drop menu to assign an available COM number to that Sapera board serial port.
- Click on the **Save Settings Now** button then the **Close** button. Reboot the computer at the prompt to enable the serial port mapping.

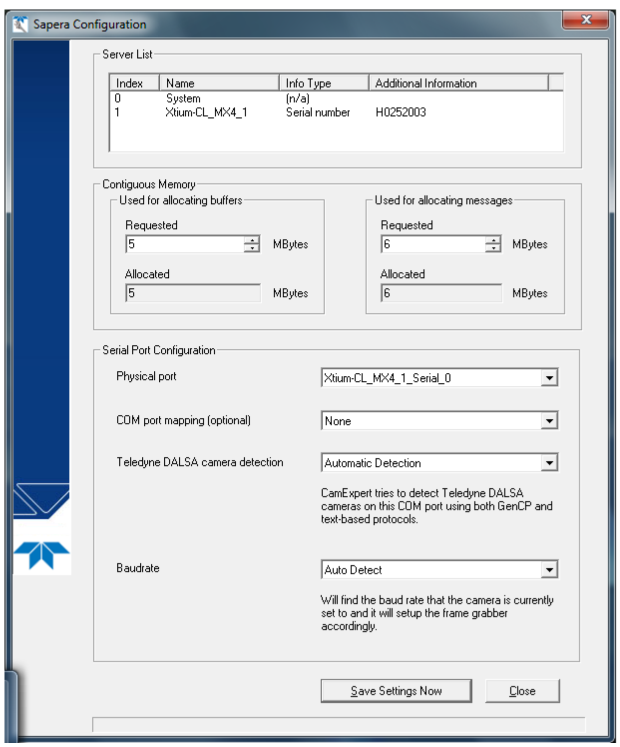


Figure 5: Sapera Configuration Program

Displaying Xtium-CL MX4 Board Information

The Device Manager program also displays information about the Xtium-CL MX4 boards installed in the system. To view board information run the program via the Windows Start Menu shortcut **Start • Programs • Teledyne DALSA • Xtium-CL MX4 Device Driver • Device Manager**.

Device Manager – Board Viewer

The following screen image shows the Device Manager program with the Information/Firmware tab active. The left window displays all Teledyne DALSA Xtium-CL MX4 boards in the system and their individual device components. The right window displays the information stored in the selected board device. This example screen shows the Xtium-CL MX4 board information.

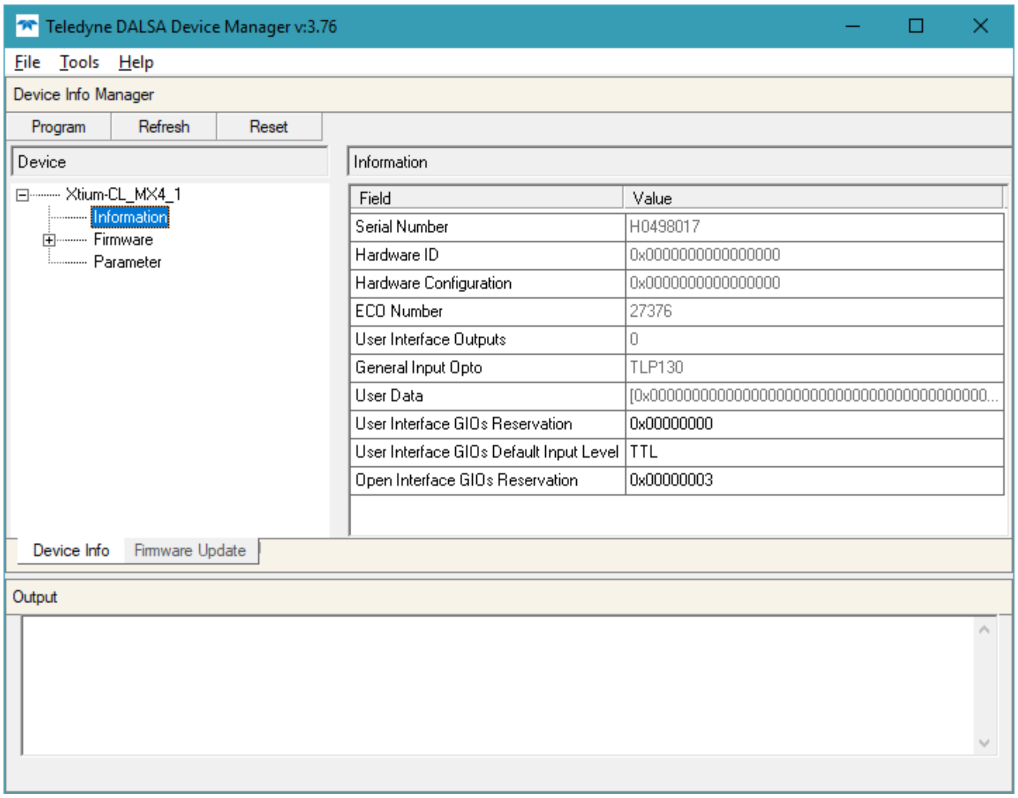


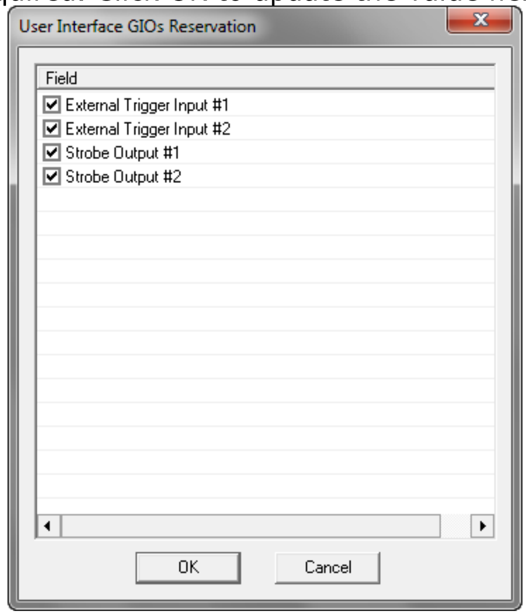
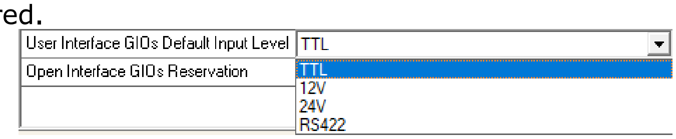
Figure 6: Board Information via Device Manager

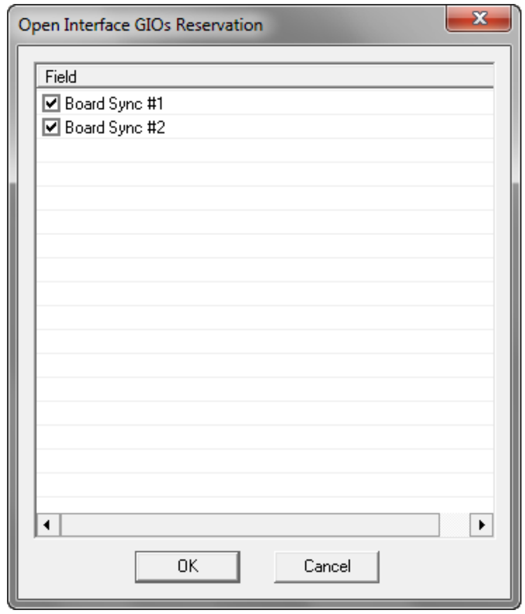
Information Field Description

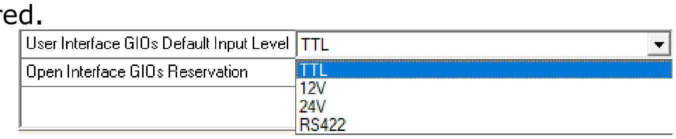
Field	Description
Serial Number	[Read-Only]: Serial Number of the board
Hardware ID	[Read-Only]: This field identifies hardware changes that affect the operation of the board. Possible values are: • **0x0000000000000000**: Rev A1 • **0x0000000000020000**: Rev A2 • **0x0000000000030000**: Rev A3 • **0x0000000000100001**: Rev B0

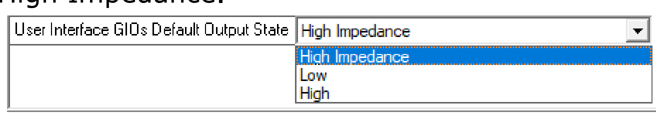
Hardware Configuration	[Read-Only]: This field will state the presence or absence of optional components.
	Possible values are:
	• **0x0000000000000000**: Rev Ax
	• **0x0000000000000003:** Rev B0
	  ○ **Bit 0:** Both Shaft Encoder RS-422 and TTL input is supported
	  ○ **Bit 1:** General Purpose Power Outputs can be set to output 5V or 12V (custom P/N)

ECO Number	[Read-Only]: Indicates the last Engineering Change Order applied to the board. **Note:** For boards Rev A1 shipped with driver 1.00, this entry will show 0.
User Interface Outputs	[Read-Only]: Number of available user interface outputs on the board. Possible values are: • **4**: Rev A1 • **8**: Rev A2/A3, Bx **Note:** For boards Rev A1 shipped with driver 1.00, this entry will show 0.
General Input Opto	[Read-Only]: Type of opto-coupler on the board. Possible values are: TLP130 (Default) **Note**: Boards shipped with driver 1.11 or earlier; 1.30 and later will show Default.
Power Output #1 Control	[Read-Only]: Controls behavior of the Power Output #1 (J1/J4 pin 14) • 12V (Default) • 5V • 12V, FVAL, Active High signal Camera #1
Power Output #2 Control	[Read-Only]: Controls behavior of the Power Output #2 (J1/J4 pin 19) • 5V (Default) • 12V • 12V, FVAL, Active High signal Camera #2
User Data	[Read/Write]: This is a 64 byte general purpose user storage area. For information on how to read/write this field at the application level, contact Teledyne DALSA Technical Support.

User Interface GIOs Reservation	[Read/Write]: Use this field to reserve User Interface GIOs for use by the acquisition module. To specifiy the GIO reservations, click on the 'Value' field to open the configuration dialog box. Disable any GIO reservations that are not required. Click OK to update the value field.  By default, boards are shipped with User Interface General Inputs 1 & 2 reserved for External Triggers and User Interface General Outputs 1 & 2 reserved for Strobe Outputs.
User Interface GIOs Default Input Level	[Read/Write]: Use this field to select the default input level of the User Interface GIOs. Click on the 'Value' field to select the input signal level detection required.  By default, boards are shipped with User Interface General Inputs set to 24V. Note that the input level can also be modified at the application level.
Open Interface GIOs Reservation	[Read/Write]: Use this field to reserve Open Interface GIOs for use by the acquisition module. To specify the open interface GIO reservations, click on the 'Value' field. Disable any GIO reservations that are not required. Click OK to update the value field.

<table>
<tr>
<td></td>
<td>

By default, boards are shipped with Open Interface GIOs 1 & 2 reserved for Board Sync 1 &</td>
</tr>
<tr>
<td>User Interface GIOs Default Output State</td>
<td>[Read/Write]: Use this field to select the default Output State of the User Interface GIOs.
Click on the ‘Value’ field to select the input signal level detection required.


By default, boards are shipped with User Interface General Outputs set to High Impedance.


Note that the output state can also be modified at the application level.</td>
</tr>
</table>

Device Information Report

Teledyne DALSA Technical Support may request device information report to aid in troubleshooting installation or operational problems. Generate the Xtium-CL MX4 device manager report file (BoardInfo.txt) by clicking **File • Save Device Info**.

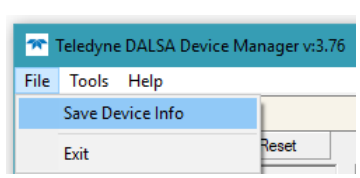


Figure 7: Device Manager File Menu Save Device Info Command

Configuring Sapera

Viewing Installed Sapera Servers

The Sapera configuration program (**Start • Programs • Teledyne DALSA • Sapera LT • Sapera Configuration**) allows the user to see all available Sapera servers for the installed Sapera-compatible boards. The **System** entry represents the system server. It corresponds to the host machine (your computer) and is the only server that should always be present.

Increasing Contiguous Memory for Sapera Resources

The **Contiguous Memory** section lets the user specify the total amount of contiguous memory (a block of physical memory, occupying consecutive addresses) reserved for the resources needed for **Sapera buffers** allocation and **Sapera messaging**. For both items, the **Requested** value dialog box shows the 'CorMem' driver default memory setting while the **Allocated** value displays the amount of contiguous memory allocated successfully. The default values will generally satisfy the needs of most applications.

The **Sapera buffers** value determines the total amount of contiguous memory reserved at boot time for the allocation of dynamic resources used for frame buffer management such as scatter-gather list, DMA descriptor tables plus other kernel needs. Adjust this value higher if your application generates any out-of-memory error while allocating host frame buffers or when connecting the buffers via a transfer object.

You can approximate the worst-case scenario amount of contiguous memory required as follows:

- Calculate the total amount of host memory used for one frame buffer
  [number of pixels per line x number of lines x 2 (*if buffer is 10/12/14 or 16 bits*)].
- Provide 200 bytes per frame buffer for Sapera buffer resources.
- Provide 64 bytes per frame buffer for metadata. Memory for this data is reserved in chunks of 64kB blocks.
- Provide 48 bytes per frame buffer for buffer management. Memory for this data is reserved in chunks of 64kB blocks.
- For each frame buffer DMA table, allocate 24 bytes + 8 bytes for each 4kB of buffer.
  For example, for a 120x50x8 image:
  120x50 = 6000 = 1.46 4kB blocks -> roundup to 2 4kB blocks.
  Therefore 24 bytes + (2 * 8 bytes) = 40 bytes for DMA tables per frame buffer.
  Memory for this data is reserved in chunks of 64kB blocks.
  If vertical flipping is enabled, one must add 16 bytes per line per buffer.
  For example, for an image 4080x3072 image: 16 bytes * 3072 = 49152 bytes.
- Note that Sapera LT reserves the 1st 5MB of its own resources, which includes the 200 bytes per frame buffer mentioned above.
- Test for any memory error when allocating host buffers. Simply use the Buffer menu of the Sapera Grab demo program (see Grab Demo Overview) to allocate the number of host buffers required for your acquisition source. Feel free to test the maximum limit of host buffers possible on your host system – the Sapera Grab demo will not crash when the requested number of host frame buffers is not allocated.
- The following calculation is an example of the amount of contiguous memory to reserve beyond 5MB with 80,000 buffers of 2048x1024x8:
  a) (80000 * 64 bytes)
  b) (80000 * 48 bytes)
  c) (80000 * (24 + (((2048*1024)/4kB) * 8))) = 323MB
  d) Total = a (rounded up to nearest 64kB) + b (rounded up to nearest 64kB) + c (rounded up to nearest 64kB).

Host Computer Frame Buffer Memory Limitations

When planning a Sapera application and its host frame buffers used, plus other Sapera memory resources, do not forget the Windows operating system memory needs.

A Sapera application using the preferred *scatter gather buffers* could consume most of the remaining system memory, with a large allocation of frame buffers. If using frame buffers allocated as a *single contiguous memory block*, Windows will limit the allocation dependent on the installed system memory. Use the Buffer menu of the Sapera Grab demo program to allocate host buffer memory until an error message signals the limit allowed by the operating system used.

Contiguous Memory for Sapera Messaging

The current value for **Sapera messaging** determines the total amount of contiguous memory reserved at boot time for messages allocation. This memory space stores arguments when a Sapera function is called. Increase this value if you are using functions with large arguments, such as arrays and experience any memory errors.

CamExpert Quick Start

Interfacing Cameras with CamExpert

CamExpert is the camera-interfacing tool for Teledyne DALSA frame grabber boards supported by the Sapera library. CamExpert is the primary tool to configure, test and calibrate your camera and imaging setup. Display tools include, image pixel value readout, image zoom, and histogram.

An important component of CamExpert is its live acquisition display window which allows immediate verification of timing or control parameters without the need to run a separate acquisition program.

Functional tools include hardware Flat Field calibration and operation support (see Flat Field Correction: Theory of Operation), plus support for either hardware based or software Bayer filter camera decoding with auto white balance calibration.

After CamExpert identifies the camera (as per the Camera Link device discovery protocol), timing parameters are displayed and the user can test image acquisition by clicking on *Grab*.

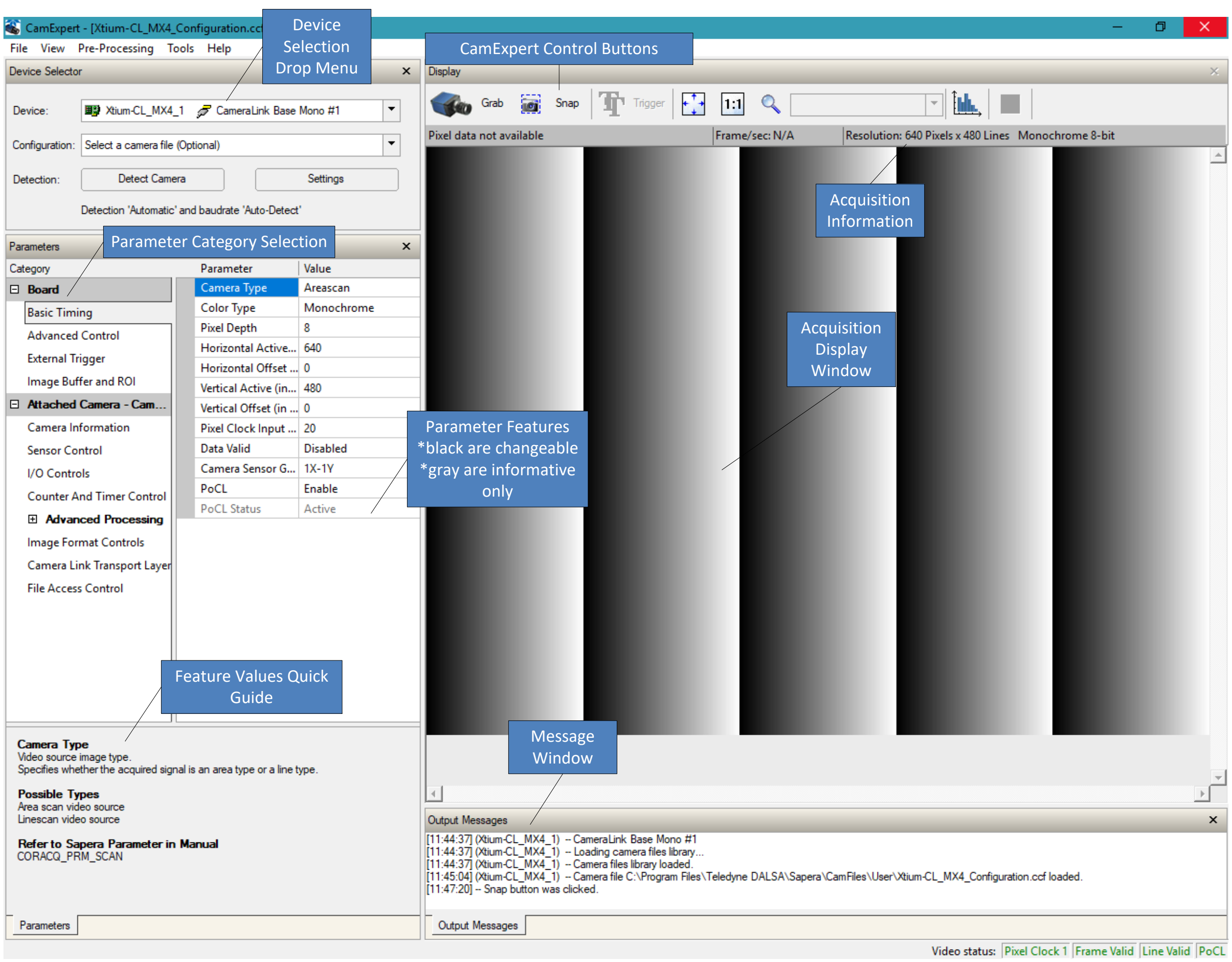


Figure 8: CamExpert Program

CamExpert groups parameters into functional categories. The parameters shown depend on the frame grabber used and what camera is connected. The parameter values are either the camera defaults or the last stored value when the camera was used.

- **Device Selector:** Two drop menus allow selection of which device and which saved configuration to use.
  - **Device:** Select which acquisition device to control and configure a camera file. Required in cases where there are multiple boards in a system and when one board supports multiple acquisition types.
  - **Configuration:** Select the timing for a specific camera model included with the Sapera installation or a standard video standard. The *User's* subsection is where user created camera files are stored.
  - **Detection:** The **Settings** button opens a menu to select the form of automatic camera detection, such as serial port text based controls or GenCP for Camera Link. The **Detect Camera** button attempts to identify the connected camera.

- **Parameter Groups:** Select a function category and change parameter values as required. Descriptions for the camera parameters change dependent on the camera.
  - **Basic Timing:** Provides or change static camera parameters.
  - **Advanced Controls:** Advanced parameters used to select various integration methods, frame trigger type, Camera Link controls, and so forth.
  - **External Trigger:** Parameters to configure the external trigger characteristics.
  - **Image Buffer and ROI:** Allows control of the host buffer dimension and format.

- **Display:** An important component of CamExpert is its live acquisition display window, which allows immediate verification of timing or control parameters without the need to run a separate acquisition program. **Grab** starts continuous acquisition (button then toggles to **Freeze** to stop). **Snap** is a single frame grab. **Trigger** is a software trigger to emulate an external source.
- **Output Messages and Video Status Bar:** Events and errors are logged for review. Camera connection status is displayed where green indicates signal present.
- **Camera Link Serial Command:** Select this Tab to open a serial command port to the camera. This allows the user to issue configuration commands if supported by the camera.

CamExpert is described more fully in the Sapera Getting started and Sapera Introduction manuals.

Sapera Camera Configuration Files

CamExpert generates the Sapera camera configuration file (*yourcamera.ccf*) based on timing and control parameters entered. When using the Sapera LT API in your imaging application, the frame grabber parameter settings can be loaded from this file. For backward compatibility with previous versions of Sapera, CamExpert also reads and writes the *.cca and *.cvi camera parameter files.

Every Sapera demo program starts with a dialog window to select a camera configuration file (for details on the included demos, see the Sapera Demo Applications section). Even when using the Xtium-CL MX4 with common video signals, a camera file is required. Therefore, CamExpert is typically the first Sapera application run after an installation. Existing .ccf files can be copied to any new board installations when similar cameras are used.

Camera Types & Files

The Xtium-CL MX4 supports digital area scan or line scan cameras using the Camera Link interface standard. Browse our web site [http://www.teledynedalsa.com/imaging/] for the latest information on Teledyne DALSA Camera Link cameras.

Camera Files Distributed with Sapera

The Sapera distribution includes camera files for a selection of Xtium-CL MX4 supported cameras. Using the Sapera CamExpert program, you may use the camera files (CCA) provided to generate a camera configuration file (CCF) that describes the desired camera and frame grabber configuration.

Teledyne DALSA continually updates a camera application library composed of application information and prepared camera files. Camera files are ASCII text, readable with Windows Notepad on any computer without having Sapera installed.

Overview of Sapera Acquisition Parameter Files (*.ccf or *.cca/*.cvi)

Concepts and Differences between the Parameter Files

There are two components to the legacy Sapera acquisition parameter file set: CCA files (also called cam-files) and CVI files (also called VIC files, i.e. video input conditioning). The files store video-signal parameters (CCA) and video conditioning parameters (CVI), which in turn simplifies programming the frame-grabber acquisition hardware for the camera in use. **Sapera LT 5.0** introduces a new camera configuration file (**CCF**) that combines the CCA and CVI files into one file.

Typically, a camera application will use a CCF file per camera operating mode (or one CCA file in conjunction with several CVI files, where each CVI file defines a specific camera-operating mode). An application can also have multiple CCA/CCF files to support different image format modes supported by the camera or sensor (such as image binning or variable ROI).

CCF File Details

A file using the ".CCF" extension, (Camera Configuration files), is the camera (CCA) and frame grabber (CVI) parameters grouped into one file for easier configuration file management. This is the default Camera Configuration file used with Sapera LT 5.0 and the CamExpert utility.

CCA File Details

Teledyne DALSA distributes camera files using the legacy ".CCA" extension, (CAMERA files), which contain all parameters describing the camera video signal characteristics and operation modes (what the camera outputs). The Sapera parameter groups within the file are:

- Video format and pixel definition
- Video resolution (pixel rate, pixels per line, lines per frame)
- Synchronization source and timing
- Channels/Taps configuration
- Supported camera modes and related parameters
- External signal assignment

CVI File Details

Legacy files using the ".CVI" extension contain all operating parameters related to the frame grabber board - what the frame grabber can actually do with camera controls or incoming video. The Sapera parameter groups within the file are:

- Activate and set any supported camera control mode or control variable.
- Define the integration mode and duration.
- Define the strobe output control.
- Allocate the frame grabber transfer ROI, the host video buffer size and buffer type (RGB888, RGB101010, MONO8, and MONO16).
- Configuration of line/frame trigger parameters such as source (internal via the frame grabber /external via some outside event), electrical format (TTL, RS-422, OPTO-isolated), and signal active edge or level characterization.

Saving a Camera File

Use CamExpert to save a camera file (*.ccf) usable with any Sapera demo program or user application.

When parameters are setup as required in CamExpert, click on **File•Save As** to save the new .ccf file. The dialog that opens allows adding details such as camera information, mode of operation, and a file name for the .ccf file. The following image is a sample for a Teledyne DALSA Falcon camera. Note the default folder where User camera files are saved.

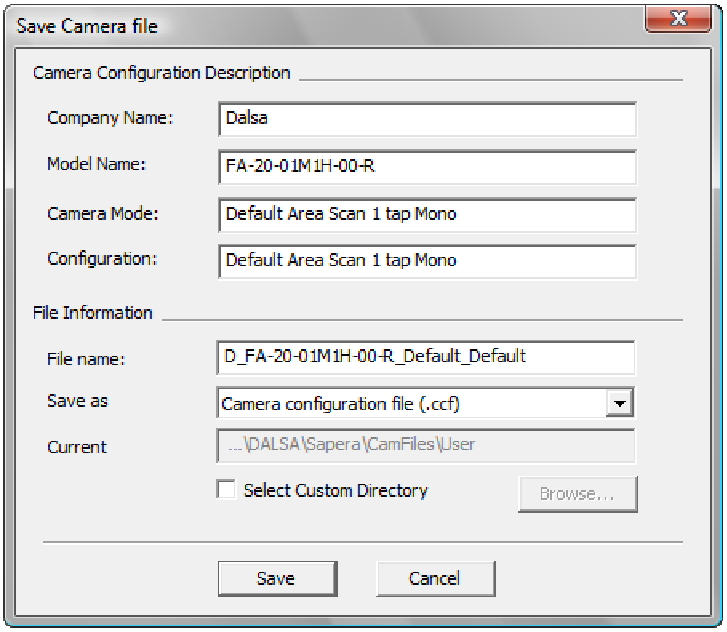


Figure 9: Saving a New Camera File (.ccf)

Camera Interfacing Check List

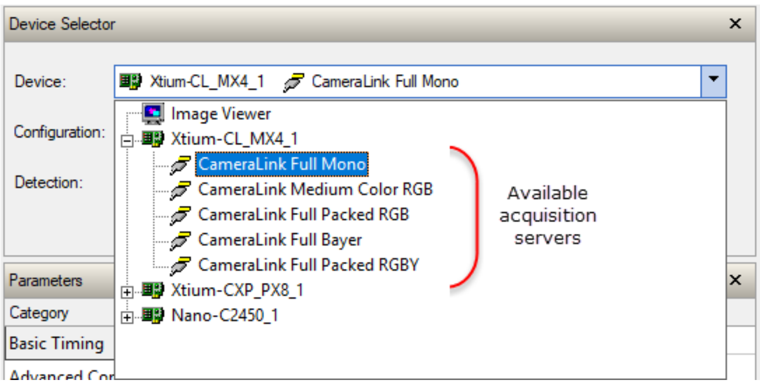
Before interfacing a camera from scratch with CamExpert:

- Confirm that Teledyne DALSA has not already published an application note with camera files [www.teledynedalsa.com].
- Confirm that the correct version or board revision of Xtium-CL MX4 is used. Confirm that the required firmware is loaded into the Xtium-CL MX4.
- Confirm that Sapera does not already have a .cca file for your camera installed on your hard disk. If there is a .cca file supplied with Sapera, then use CamExpert to generate the .ccf file with default parameter values matching the frame grabber capabilities.
- Check if the Sapera installation has a similar type of camera file. A similar .cca file can be loaded into CamExpert and modified to match timing and operating parameters for your camera, and lastly save them as Camera Configuration file (.ccf).
- Finally, if there is no file for your camera, run CamExpert after installing Sapera and the acquisition board driver, select the board acquisition server, and manually enter the camera parameters.

Using CamExpert with Xtium-CL MX4

The Sapera CamExpert tool is the interfacing tool for Xtium-CL MX4 frame grabbers and connected cameras; it is supported by the Sapera library and hardware. CamExpert allows a user to test frame grabber and camera functions. Additionally CamExpert saves the frame grabber settings configuration as individual camera parameter files on the host system (*.ccf).

When an acquisition server is selected, CamExpert only presents parameters supported by the selected device.



The three Xtium-CL MX4 firmware options provide the following acquisition servers:

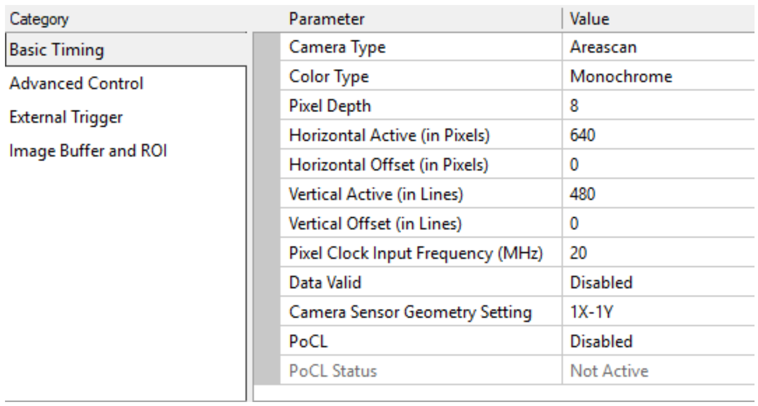
Firmware	Acquisition Servers
1 x Full Camera Link (default configuration)	Xtium-CL_MX4_1 CameraLink Full Mono CameraLink Medium Color RGB CameraLink Full Packed RGB CameraLink Full Bayer CameraLink Full Packed RGBY
80-Bits Camera Link	Xtium-CL_MX4_1 CameraLink 10-Tap/8-Bit Mono CameraLink 8-Tap/10-Bit Mono CameraLink 80-Bit Packed RGB CameraLink 80-Bit Packed/8-Bit Bi-Color CameraLink 10-Tap/8-Bit Bayer CameraLink 8-Tap/10-Bit Bayer
2 x Base Camera Link	Xtium-CL_MX4_1 CameraLink Base Mono #1 CameraLink Base Mono #2 CameraLink Base Color RGB #1 CameraLink Base Color RGB #2 CameraLink Base Bayer #1 CameraLink Base Bayer #2

Depending on the selected server, different parameters may be displayed. For example, with an RGB acquisition server, the Color Type parameter is not displayed since its value is not configurable.

For more information, see the Sapera Servers & Resources section.

Basic Timing Category

The Basic Timing category groups parameters such as camera type, the active image size, and other settings related to basic timing.



Parameter Descriptions

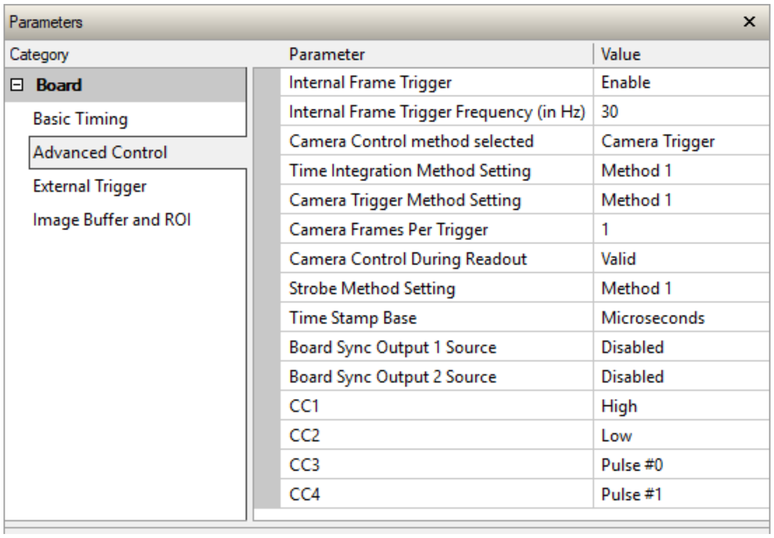
The following table describes the CamExpert Basic Timing category of Sapera LT parameters. Acquisition server notes, if applicable, indicate if parameter availablility or supported values are dependent on the selected frame grabber acquisition server and acquisition device.

Display Name	Parameter	Description	Notes
Camera Type	CORACQ_PRM_SCAN	Video source image type. Possible values are areascan or line scan.	Not shown for Bayer servers (areascan only).
Color Type	CORACQ_PRM_VIDEO	Sets the color format of the input source.	Not shown for RGB or Bayer servers. Monochrome servers support: Monochrome Bayer mosaic
Pixel Depth	CORACQ_PRM_PIXEL_DEPTH	Pixel depth (bits per pixel) of the input source.	Not shown for RGB servers. Monchrome servers support: 8, 10, 12, 14 or 16 bit Bayer servers support: 8, 10 or 12 bit
Horizontal Active (in Pixels)	CORACQ_PRM_HACTIVE	Sets the horizontal camera resolution in pixels. This corresponds to the visible part of the image from the camera.	For application server specifc support, refer to the parameter CORACQ_PRM_HACTIVE description.
Horizontal Offset (in Pixels)	CORACQ_PRM_HBACK_INVALID	Sets the number of invalid pixels before the active portion of the line, in pixels per tap. Valid range is 0-65535.	
Vertical Active (in Lines)	CORACQ_PRM_VACTIVE	Sets the vertical camera resolution in lines per frame. This corresponds to the visible part of the image from the camera. Valid range is 1-16777215.	Not shown for linescan cameras.
Vertical Offset (in Lines)	CORACQ_PRM_VBACK_INVALID	Sets the number of invalid lines before the active portion of the line. Valid range is 0-16777215.	Not shown for linescan cameras.

Pixel Clock Input Frequency (MHz)	CORACQ_PRM_PIXEL_CLK_EXT	Specifies the external pixel clock frequency, in MHz. Valid range is 20-85MHz.	
Data Valid	CORACQ_PRM_DATA_VALID_ENABLE	Specifies if the acquisition board uses the camera data valid signal. Boolean parameter (TRUE or FALSE).	
Camera Sensor Geometry Setting	CORACQ_PRM_TAPS CORACQ_PRM_TAP_OUTPUT CORACQ_PRM_CAMLINK_CONFIGURATION	Defines the number of taps output and how multi-tap data is output by the camera.	For application server specifc support, refer to the parameter CORACQ_PRM_x descriptions.
PoCL	CORACQ_PRM_POCL_ENABLE	Enables/disables sending power through the Camera Link cable. Boolean parameter (TRUE or FALSE).	
PoCL Status	CORACQ_PRM_SIGNAL_STATUS	Status of POCL signals connected to the acquisition device. Possible values are Active or Not Active.	

Advanced Control Category

The Advanced Control category groups parameters for configuring camera control signals, board sync outputs and other advanced settings.



Parameter Descriptions

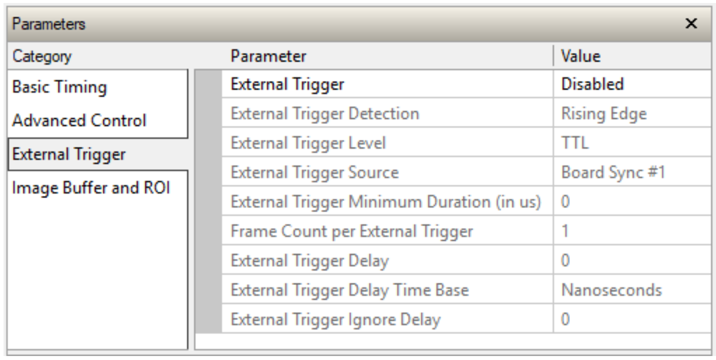
The following table describes the CamExpert Advanced Control category of Sapera LT parameters. Acquisition server notes, if applicable, indicate if parameter availablility or supported values are dependent on the selected frame grabber acquisition server and acquisition device.

Display Name	Parameter	Description	Notes
Internal Frame Trigger	CORACQ_PRM_INT_FRAME_TRIGGER_ENABLE	Enables/disables the acquisition device's internal frame trigger. Boolean parameter (TRUE or FALSE).	Applies to areascan cameras only.
Internal Frame Trigger Frequency (in Hz)	CORACQ_PRM_INT_FRAME_TRIGGER_FREQ	Internal frame trigger frequency in Hz. Set to the required frame rate when using internal frame trigger to control camera acquisition. Valid range is 0.001-10000Hz.	
Line Sync Source	CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE CORACQ_PRM_INT_LINE_TRIGGER_ENABLE CORACQ_PRM_SHAFT_ENCODER_ENABLE	Selects the line trigger source for linescan cameras, unless free-running.	Applies to linescan cameras only.
Interal Line Trigger Frequency (in Hz)	CORACQ_PRM_INT_LINE_TRIGGER_FREQ	Sets the internal line trigger frequency, in Hz. Applies only when the Line Sync Source is set to Internal Line Trigger.	Applies to linescan cameras only.
Camera Line Trigger Frequency Min (in Hz)	CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MIN	Sets the camera's minimum line trigger frequency. Minimum value is 1Hz.	Applies to linescan cameras only.
Camera Line Trigger Frequency Max (in Hz)	CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MAX	Sets the camera's maximum line trigger frequency. Maximum value is 10000000 Hz.	Applies to linescan cameras only.
Camera Control method selected	CORACQ_PRM_TIME_INTEGRATE_ENABLE CORACQ_PRM_CAM_TRIGGER_ENABLE CORACQ_PRM_LINE_TRIGGER_ENABLE	Enables or disables an available camera control method. Each supported control method has one or more operating modes to choose from; refer to the parameters: Camera Trigger Method Setting Time Integration Method Setting.	

Time Integration Method Setting	CORACQ_PRM_TIME_INTEGRATE_METHOD CORACQ_PRM_TIME_INTEGRATE_DELAY CORACQ_PRM_TIME_INTEGRATE_PULSE0_DELAY CORACQ_PRM_TIME_INTEGRATE_PULSE1_DELAY CORACQ_PRM_TIME_INTEGRATE_PULSE0_DURATION CORACQ_PRM_TIME_INTEGRATE_PULSE1_DURATION CORACQ_PRM_TIME_INTEGRATE_PULSE0_POLARITY CORACQ_PRM_TIME_INTEGRATE_PULSE1_POLARITY	When the Camera Control method is Time Integration, select and configure the control method required. Click on the parameter field to open the configuration dialog.	
Camera Trigger Method Setting	CORACQ_PRM_CAM_TRIGGER_METHOD	When an asynchronous trigger pulse to a camera is required, select and configure the required method.	
Line Integration Method Setting	CORACQ_PRM_LINE_INTEGRATE_METHOD	Sets the method for controlling the camera's line integration.	Applies to linescan cameras only
Line Trigger Method Setting	CORACQ_PRM_LINE_TRIGGER_METHOD	Sets the method for line trigger pulse output.	Applies to linescan cameras only
Camera Frames Per Trigger	CORACQ_PRM_CAM_FRAMES_PER_TRIGGER	Specifies the number of frames output by the camera per trigger. Valid only for area scan cameras. Valid range is 1-262142.	
Camera Control During Readout	CORACQ_PRM_CAM_CONTROL_DURING_READOUT	Specifies if the camera control signals can be sent during the readout of a frame. Possible values are Valid or Invalid.	
Strobe Method Setting	CORACQ_PRM_STROBE_METHOD CORACQ_PRM_STROBE_ENABLE CORACQ_PRM_STROBE_DELAY CORACQ_PRM_STROBE_DURATION CORACQ_PRM_STROBE_LEVEL CORACQ_PRM_STROBE_POLARITY	When a strobe output signal from the acquisition board is required, select and configure the control method required. Note, method 1 is only available for areascan camera type; method 3 for line scan only.	
Line Trigger Auto Delay	CORACQ_PRM_LINE_TRIGGER_AUTO_DELAY	Enables delaying line triggers to a camera based on the selected method. Used to avoid over-triggering a camera.	Applies to linescan cameras only
Time Stamp Base	CORACQ_PRM_TIME_STAMP_BASE	Sets the counter stamp time base. Possible values are: • Microseconds • Line Counts • External line trigger or shaft encoder • 100 Nanoseconds	
Board Sync Output 1 Source	CORACQ_PRM_BOARD_SYNC_OUTPUT1_SOURCE	Specifies the signal to output on board sync output 1. This parameter permits the synchronization of two acquisition devices using a signal from one acquisition device and synching the second acquisition device with it.	
Board Sync Output 2 Source	CORACQ_PRM_BOARD_SYNC_OUTPUT2_SOURCE	Specifies the signal to output on board sync output 2. This parameter permits the synchronization of two acquisition devices using a signal from one acquisition device and synching the second acquisition device with it.	
CC1 to CC4	CORACQ_PRM_CAM_IO_CONTROL	General purpose camera control. Four LVDS pairs are reserved for general purpose camera control. They are defined as camera inputs and frame grabber outpus. Camera manufacturers can define these signals to meet their needs for a particular product.	

External Trigger Category

The External category groups parameters for configuring an external trigger for controlling image acquisition.



Parameter Descriptions

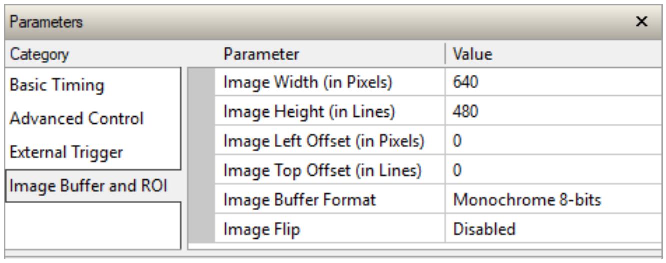
The following table describes the CamExpert External Trigger category of Sapera LT parameters. Acquisition server notes, if applicable, indicate if parameter availablility or supported values are dependent on the selected frame grabber acquisition server and acquisition device.

Display Name	Parameter	Description
External Trigger	CORACQ_PRM_EXT_TRIGGER_ENABLE	Enables/disables external trigger on the acquisition board. When enabled, the acquisition board acquires an image frame from the camera after receiving the trigger. Boolean parameter (TRUE or FALSE). Note: Applies to area scan cameras only.
External Trigger Detection	CORACQ_PRM_EXT_TRIGGER_DETECTION	Defines the signal detected that generates an external trigger event to the acquisition device. Two types of trigger are available: *Level Trigger: Active Low / High* Logic level (Low/High) on the trigger input enables continuous image capture until the trigger input is set to opposite logic . *Edge Trigger: Rising / Falling edge* Edge transition of a trigger pulse captures one image frame.
External Trigger Level	CORACQ_PRM_EXT_TRIGGER_LEVEL	Specifies the electrical level of the external trigger connected to the acquisition board. Possible values: TTL single-ended logic signal RS-422 balanced logic signal 12V single-ended logic signal 24V single-ended logic signal

External Trigger Source	CORACQ_PRM_EXT_TRIGGER_SOURCE	Specifies the physical input source the external frame trigger is connected to or which trigger input is used on the acquisition device. Note: to assign the external trigger source to a GPIO it must be reserved; By default, boards are shipped with User Interface General Inputs 1 & 2 reserved for External Triggers and User Interface General Outputs 1 & 2 reserved for Strobe Outputs. Refer to User Interface GIOs Reservation for more information on using the Teledyne DALSA Device Manager tool to reserve GPIOs.
External Trigger Minumum Duration (in µs)	CORACQ_PRM_EXT_TRIGGER_DURATION	Minimum external trigger pulse duration (in µs), needed for the pulse to be acknowledged by the acquisition device. If the duration of the pulse is shorter, the pulse is ignored. This feature is useful for trigger pulse debouncing. If the value is ‘0’, no validation is performed
Frame Count per External Trigger	CORACQ_PRM_EXT_TRIGGER_FRAME_COUNT	Number of images to acquire upon receiving an external trigger. Valid range is 1-262142. Note, infinite frame count (-1) is not supported.
External Trigger Delay	CORACQ_PRM_EXT_TRIGGER_DELAY	Sets the delay between the reception of the trigger signal and the start of the image acquisition. Units are specified by the External Trigger Delay Time Base parameter.
External Trigger Delay Time Base	CORACQ_PRM_EXT_TRIGGER_DELAY_TIME_BASE	Sets the external trigger delay time base. Possible values: ns — nanoseconds us — microseconds ms — milliseconds line — line counts line trigger — external line trigger or shaft encoder pulse counts (after drop and/or multiply factors) shaft encoder — shaft encoder pulse counts (after drop and/or multiply factors) frame — image frame counts
External Trigger Ignore Delay	CORACQ_PRM_EXT_TRIGGER_IGNORE_DELAY	Sets the time delay, in µsec, where if another external trigger occurs, it is ignored. Valid range is 0-85899344. The start of the delay (time '0') is the end of the next vertical sync for analog cameras, or the beginning of the next frame valid for digital cameras, following a valid external trigger.

Image Buffer and ROI Category

The Image Buffer and ROI category groups parameters for the configuring the image buffer format, size and offset settings, as well as image flipping.



Parameter Descriptions

The following table describes the CamExpert Image Buffer and ROI category of Sapera LT parameters. Acquisition server notes, if applicable, indicate if parameter availablility or supported values are dependent on the selected frame grabber acquisition server and acquisition device.

Display Name	Parameter	Description	Notes
Image Width (in Pixels)	CORACQ_PRM_CROP_WIDTH	Cropped width of the acquisition image, in pixels; this parameter defines the width of the image transferred to the frame buffer. The maximum width is the active horizontal of the image source (see the Horizontal Active parameter in the Basic Timing category). Cropping increments depend on the selected acquisition server; CamExpert automatically adjusts numerical entries to valid increments.	Note: image data is not scaled.
Image Height (in Lines)	CORACQ_PRM_CROP_HEIGHT	Cropped height of the acquisition image, in lines; this parameter defines the vertical dimension of the image transferred to the frame buffer. The maximum height is the active vertical width of the image source (see the Vertical Active parameter in the Basic Timing category). Cropping increments depend on the selected acquisition server; CamExpert automatically adjusts numerical entries to valid increments.	Note: image data is not scaled.
Image Left Offset (in Pixels)	CORACQ_PRM_CROP_LEFT	Number of pixels to crop from the left side of the acquisition image before transfer to the frame buffer. The maximum left offset is the active horizontal width of the image source less one increment step. Cropping increments depend on the selected acquisition server; CamExpert automatically adjusts numerical entries to valid increments.	Note: image data is not scaled.

Image Top Offset (in Lines)	CORACQ_PRM_CROP_TOP	Number of lines to crop from the top of the acquisition image before transfer to the frame buffer. The maximum top offset is the active vertical height of the image source less one increment step. Cropping increments are acquisition hardware dependent; CamExpert automatically adjusts numerical entries to valid increments.	Note: image data is not scaled.
Image Buffer Format	CORACQ_PRM_OUTPUT_FORMAT	Data format for the acquisition image transfer to the frame buffer.	The data buffer format is dependent on the selected acquisition server; for details refer to the CORACQ_PRM_OUTPUT_FORMAT parameter description
Image Flip	CORACQ_PRM_FLIP	Enables real-time on-board horizontal image flip function. The Xtium-CL MX4 also supports a vertical flip operation using CORXFER_PRM_FLIP.	Note: Full Packed RGBY acquisition server does not support the image flip operation.
Acquisition Frame Length	CORACQ_PRM_FRAME_LENGTH	Specifies if the images output by the acquisition device have a fixed or variable frame length.	Only available using Camera Link Full Packed RGBY server.

Using the Flat Field Correction Tool

Flat Field Correction is the process of eliminating small gain differences between pixels in a sensor array. That sensor when exposed to a uniformly lit field will have no gray level differences between pixels when calibrated flat field correction is applied to the image. The CamExpert Flat Field tool functions with hardware supporting flat field processing.

Xtium-CL MX4 Flat Field Support

The Xtium-CL MX4 supports hardware based real-time Flat Field Correction when used with a monochrome video source. The Xtium-CL MX4 supports two methods for pixel replacement:

- Neighborhood Replacement: a bad pixel is replaced with the average of its 2 neighbors on the same video line.
- 3x2 Cluster Replacement: a bad pixel is replaced with the average of its 5 neighbors, its two line neighbors and the 3 pixel neighbors from the line above. Support for this feature using Sapera Classes and CamExpert will be available in Sapera LT 8.20, therefore contact Teledyne DALSA Technical Support for any inquiry regarding this feature. Note that this process requires a cluster map file defining bad pixels, provided by the camera manufacturer.
- Note that the MX4 Flat Field algorithm handles all cases of bad pixels being on the frame edge or where neighboring pixels are also bad.

Loading the Required Camera File

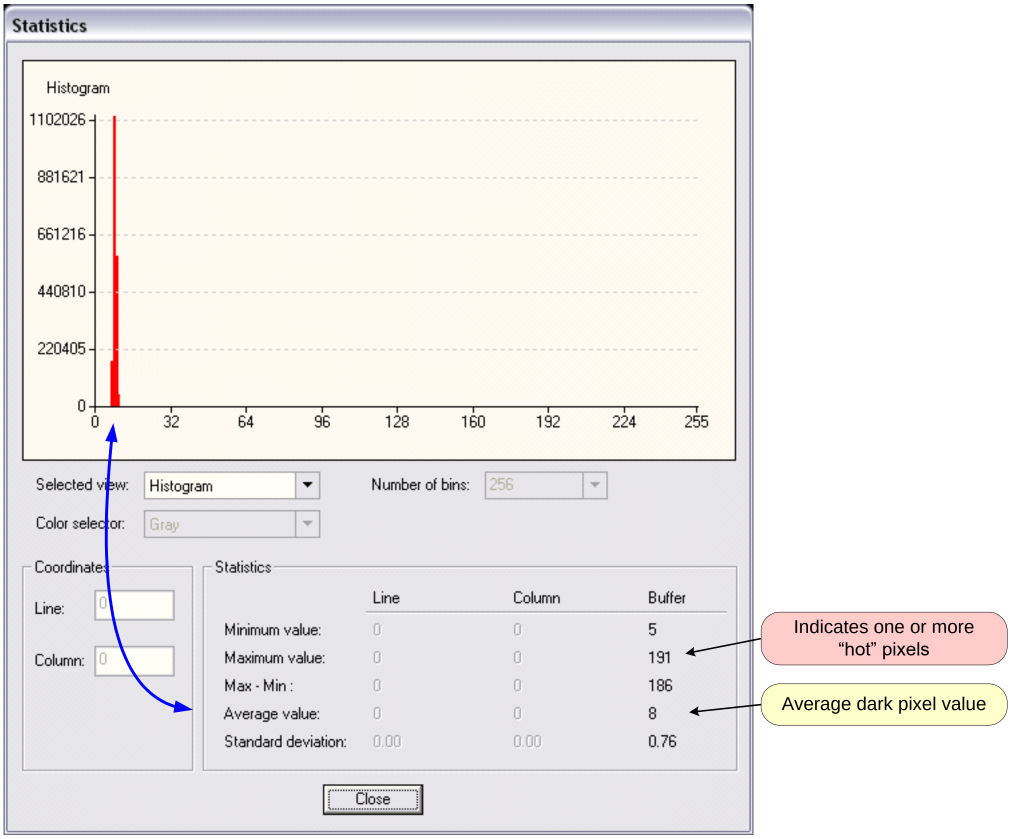
Select the required camera configuration file for the connected camera. Verify the acquisition with the live grab function. Make camera adjustments to get good images.

Set up Dark and Bright Acquisitions with the Histogram Tool

Before performing calibration, verify the acquisition with a live grab. Also at this time make preparations to grab a flat light gray level image, required for the calibration, such as a clean evenly lighted white wall or non-glossy paper with the lens slightly out of focus. Ideally a controlled diffused light source aimed directly at the lens should be used. Note the lens iris position for a bright but not saturated image. Additionally check that the lens iris closes well or have a lens cover to grab the dark calibration image.

Verify a Dark Acquisition

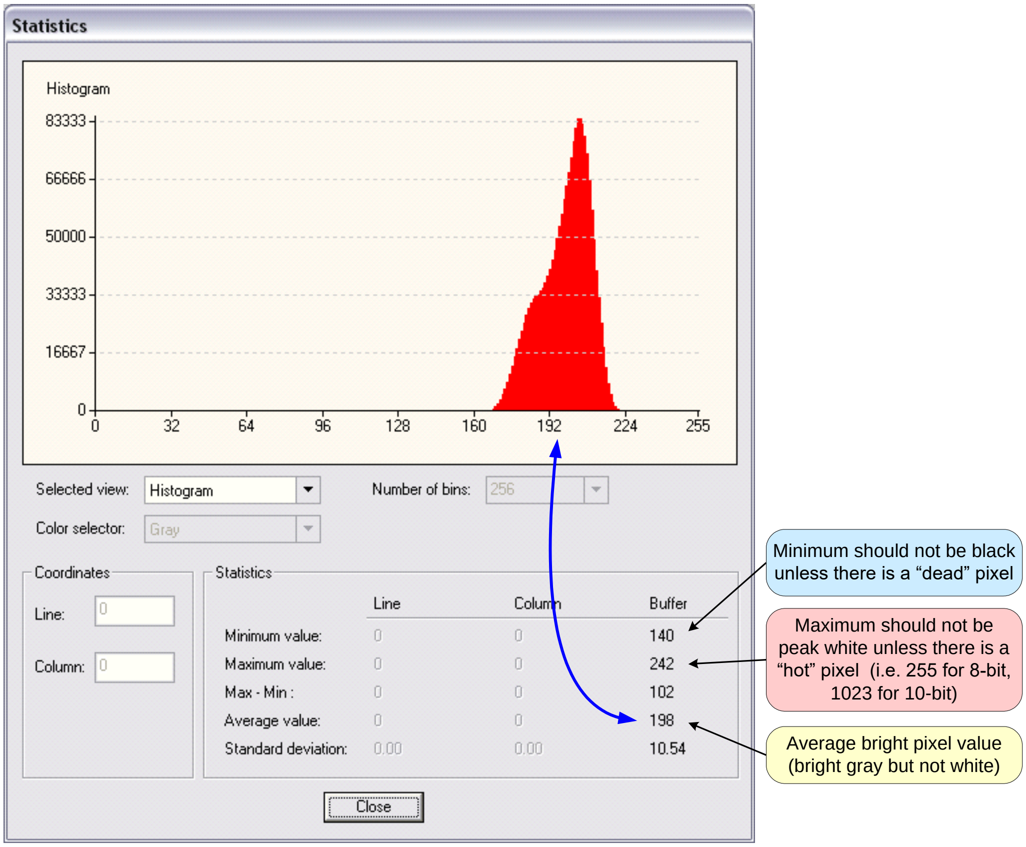
Close the camera lens iris and cover the lens with a lens cap. Using CamExpert, click on the grab button and then the histogram button. The following figure shows a typical histogram for a very dark image (8-bit acquisition).



Important: In this example, the **average** pixel value for the frame is close to black. Also note that most sensors will show a much higher maximum pixel value due to one or more "hot pixels". The sensor specification accounts for a small number of hot or stuck pixels (pixels that do not react to light over the full dynamic range specified for that sensor).

Verify a Bright Acquisition

Aim the camera at a diffused light source or evenly lit white wall with no shadows falling on it. Using CamExpert, click on the grab button and then the histogram button. Use the lens iris to adjust for a bright gray approximately around a pixel value of 200 (for 8-bit pixels). The following figure shows a typical histogram for a bright gray image.



Important: In this example, the **average** pixel value for the frame is bright gray. Also note that sensors may show a much higher maximum or a much lower minimum pixel value due to one or more "hot or dead pixels". The sensor specification accounts for a small number of hot, stuck, or dead pixels (pixels that do not react to light over the full dynamic range specified for that sensor).

Once the bright gray acquisition setup is done, note the camera position and lens iris position so as to be able to repeat it during the calibration procedure.

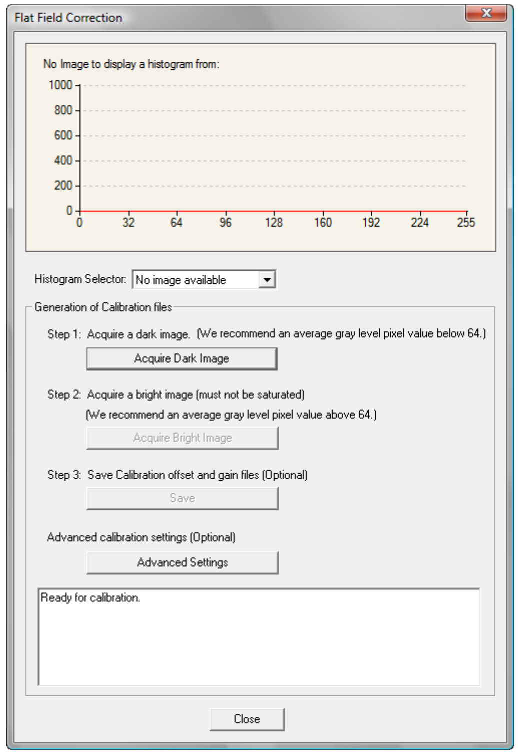
Flat Field Correction Calibration Procedure

Calibration is the process of taking two reference images, one of a black field – one of a light gray field (not saturated), to generate correction data for images captured by the CCD. Each CCD pixel data is modified by the correction factor generated by the calibration process, so that each pixel now has an identical response to the same illumination.

Start the Flat Field calibration tool via the CamExpert menu bar:
Tools • Flat Field Correction • Calibration.

Flat Field Calibration Window

The Flat Field calibration window provides a three step process to acquire two reference images and then save the flat field correction data for the camera used. To aid in determining if the reference images are valid, a histogram tool is provided so that the user can review the images used for the correction data.



- Setup the camera to capture a uniform black image. Black paper with no illumination and the camera lens' iris closed to minimum can provide such a black image.
- Click on **Acquire Black Image**. The flat field demo will grab a video frame, analyze the pixel gray level spread, and present the statistics. The desired black reference image should have pixel values less then 20. If acceptable accept the image as the black reference.
- Setup the camera to acquire a uniform white image (but not saturated white). Even illumination on white paper can be used, with a gray level of 128 minimum. It is preferable to prepare for the white level calibration before the calibration procedure.
- Click on **Acquire White Image**. The flat field demo will grab a video frame, analyze the pixel gray level spread, and present the statistics. The captured gray level for all pixels should be greater than 128. If acceptable accept the image as the white reference.
- Click on **Save**. The flat field correction data is saved as a TIF image with a file name of your choice (such as camera name and serial number).

Using Flat Field Correction

From the CamExpert menu bar enable Flat Field correction (**Tools • Flat Field Correction • Enable**). Now when doing a live grab or snap, the incoming image is corrected by the current flat field calibration data for each pixel.

Use the menu function **Tools • Flat Field Correction • Load** to load in a flat field correction image from a previous saved calibration data. CamExpert allows saving and loading calibration data for all cameras used with the imaging system.

Using the Bayer Filter Tool

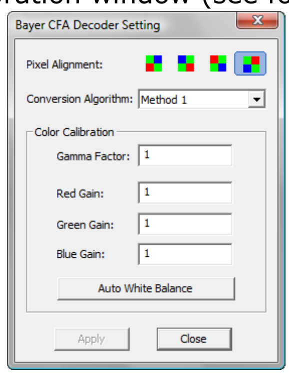
CamExpert supports the use of Bayer Filter cameras by providing a tool to select the Bayer filter mosaic pattern and to perform an auto white balance. Color calibration can then be manually fine tuned with RGB gain and gamma adjustments.

The CamExpert Bayer filter tool supports using both software or hardware based decoding. With boards that have Bayer filter decoding in hardware, CamExpert directly controls the hardware for high performance real-time acquisitions from Bayer filter cameras. When standard acquisition boards are used, CamExpert performs software Bayer filter decoding using the host system processor.

Bayer Filter White Balance Calibration Procedure

The following procedure uses the hardware Bayer filter support (Bayer Decoder firmware loaded) and any supported Bayer color camera. It is assumed that CamExpert was used to generate a camera file with correct camera timing parameters.

- On the CamExpert menu bar, click on **Tools • Bayer Filter**. The following menu should show **Hardware** selected by default when the frame grabber has Bayer support.
- Select **Setting** to access the color calibration window (see following figure).



- Click **Grab** to start live acquisition.
- Aim and focus the camera. The camera should see an area of white or place white paper in front of the object being imaged.
- Click on one of the four Bayer pixel alignment patterns to match the camera (best color before calibration). Typically the CamExpert default is correct for a majority of cameras.
- Adjust the lens iris to reduce the exposure brightness so that the white image area is now darker. Make certain that no pixel in the white area is saturated.
- Using the mouse left button, click and drag a ROI enclosing a portion of the white area.
- Click on the **Auto White Balance** button. CamExpert will make RGB gain adjustments.
- Open the camera iris to have a correctly exposed image.
- Review the image for color balance.
- Manually make additional adjustments to the RGB gain values. Fine tune the color balance to achieve best results. Adjust the gamma factor to optionally improve the display.
- Stop the live acquisition and save the camera file (which now contains the Bayer RGB calibration information). Note that the gamma factor is not save because it is not a Sapera parameter but only a display tool.

Using the Bayer Filter

A Sapera application, when loading the camera file parameters, will have the RGB gain adjustment values. The application can incorporate a calibration menu for RGB adjustments as required.

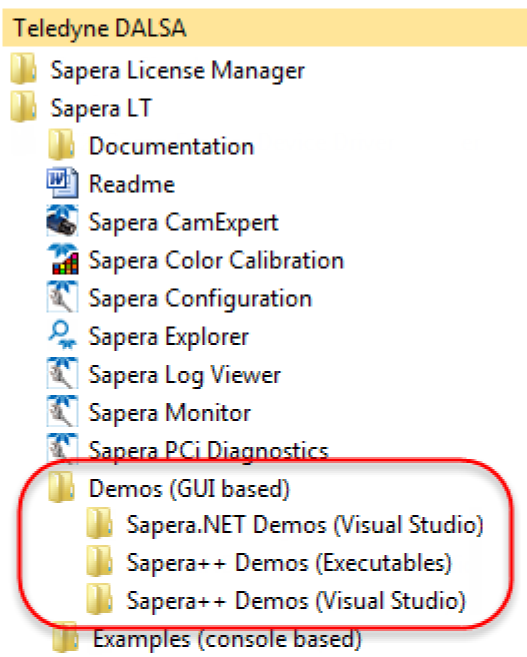
Sapera Demo Applications

Grab Demo Overview

The Grab Demo program demonstrates the basic acquisition functions included in the Sapera library. The program either allows you to acquire images, in continuous or in one-time mode, while adjusting the acquisition parameters. The program code may be extracted for use within your own application.

The Grab Demo is available as a compiled binary; source code is provided for both C++ and .NET projects using Visual Studio 2005/2008/2010/2012/2013/2015.

All demos are available through the Start menu.



Grab Demo Workspace Details

Program file	**...\\...\\Sapera\\Demos\\Binaries\\GrabDemo.exe**
Visual C++ Solution	**...\\...\\Sapera\\Demos\\Classes\\Vc\\SapDemos_2005.sln** **...\\...\\Sapera\\Demos\\Classes\\Vc\\SapDemos_2008.sln** **...\\...\\Sapera\\Demos\\Classes\\Vc\\SapDemos_2010.sln** **...\\...\\Sapera\\Demos\\Classes\\Vc\\SapDemos_2012.sln** **...\\...\\Sapera\\Demos\\Classes\\Vc\\SapDemos_2013.sln** **...\\...\\Sapera\\Demos\\Classes\\Vc\\SapDemos_2015.sln**
Visual .NET Solution	**...\\...\\Sapera\\Demos\\NET\\SapDemos_2005.sln** **...\\...\\Sapera\\Demos\\NET\\SapDemos_2008.sln** **...\\...\\Sapera\\Demos\\NET\\SapDemos_2010.sln** **...\\...\\Sapera\\Demos\\NET\\SapDemos_2012.sln** **...\\...\\Sapera\\Demos\\NET\\SapDemos_2013.sln** **...\\...\\Sapera\\Demos\\NET\\SapDemos_2015.sln**
Remarks	This demo is based on Sapera LT classes. See the Sapera User's and Reference manuals for more information.

Using the Grab Demo

Server Selection

Run the grab demo from the start menu:

Start•Programs•Sapera LT•Demos•Frame Grabbers•Grab Demo.

The demo program first displays the acquisition configuration menu. The first drop menu displayed permits selecting from any installed Sapera acquisition servers (installed Teledyne DALSA acquisition hardware using Sapera drivers). The second drop menu permits selecting from the available input devices present on the selected server.

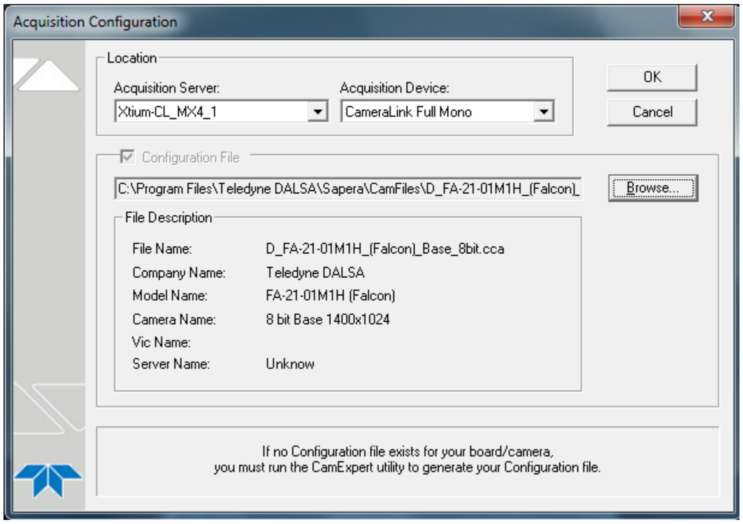


Figure 10: Grab Demo – Server Selection

CCF File Selection

Use the acquisition configuration menu to select the required camera configuration file for the connected camera. Sapera camera files contain timing parameters and video conditioning parameters. The default folder for camera configuration files is the same used by the CamExpert utility to save user generated or modified camera files.

Use the Sapera CamExpert utility program to generate the camera configuration file based on timing and control parameters entered. The CamExpert live acquisition window allows immediate verification of those parameters. CamExpert reads both Sapera *.cca and *.cvi for backward compatibility with the original Sapera camera files.

Grab Demo Main Window

The Grab Demo program provides basic acquisition control for the selected frame grabber. The loaded camera file (.ccf) defines the Frame buffer defaults.

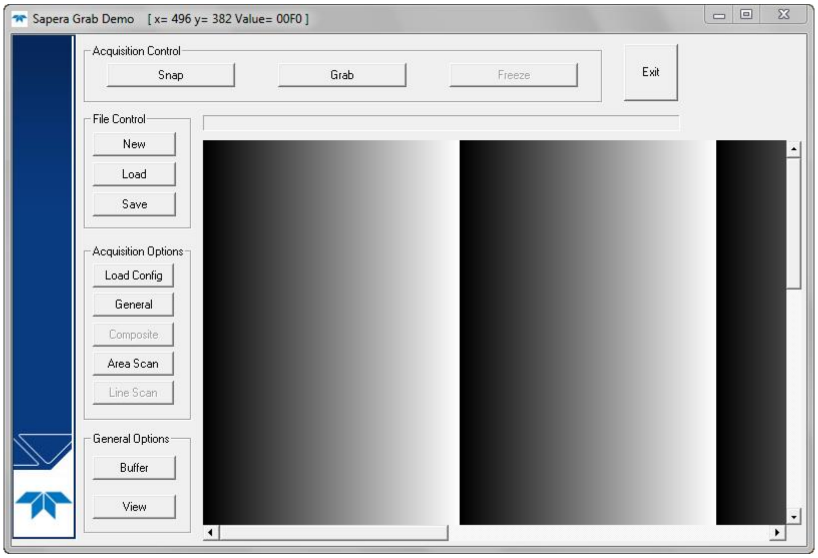


Figure 11: Grab Demo Main Window

Refer to the Sapera LT User's Manual (OC-SAPM-USER), in section "Demos and Examples – Acquiring with Grab Demo", for more information on the Grab Demo and others provided with Sapera LT.

Xtium-CL MX4 Reference

Block Diagram

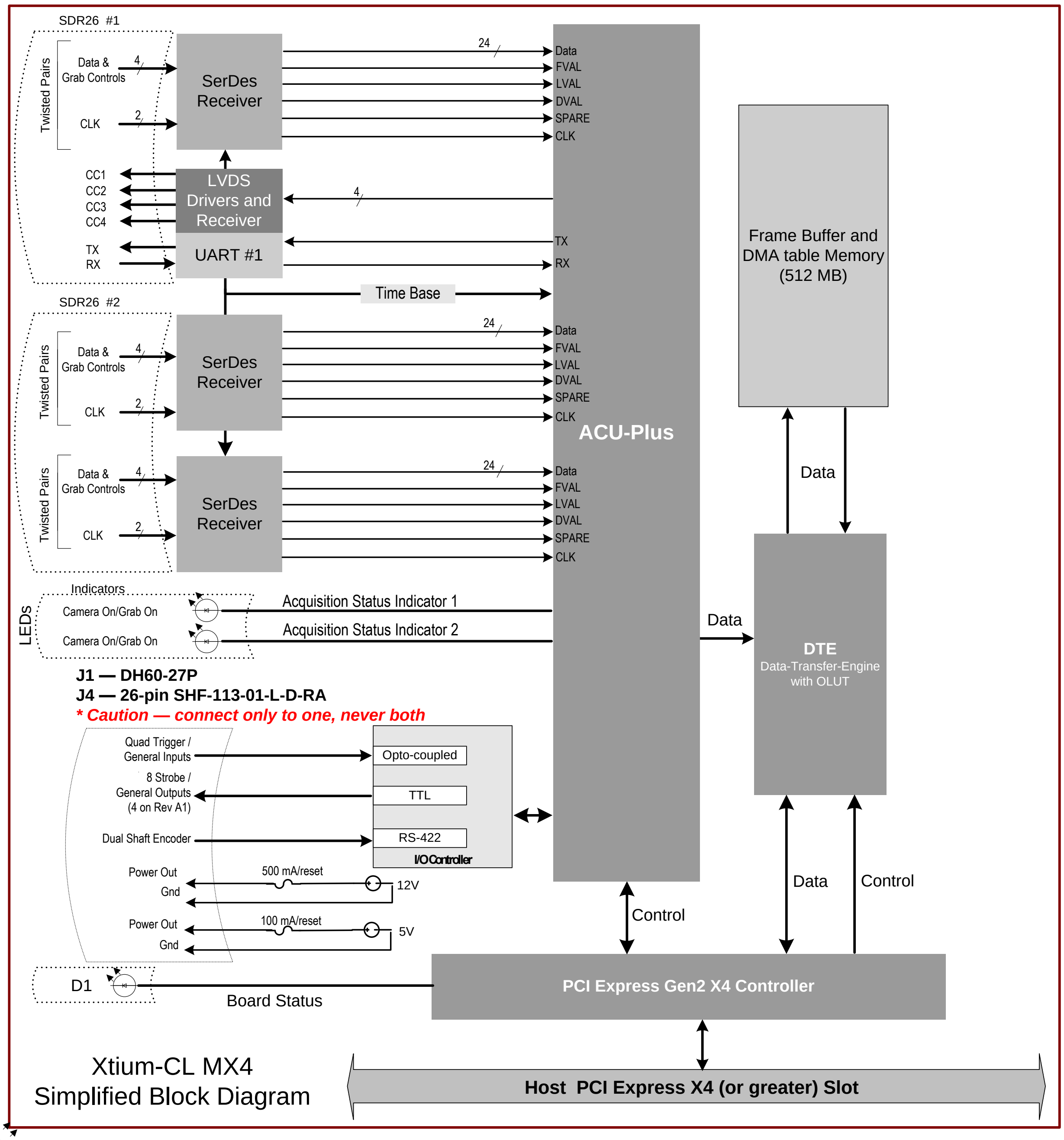


Figure 12: Xtium-CL MX4 Model Block Diagram

Xtium-CL Flow Diagram

The following diagram represents the sequence in which the camera data acquired is processed through the Xtium-CL.

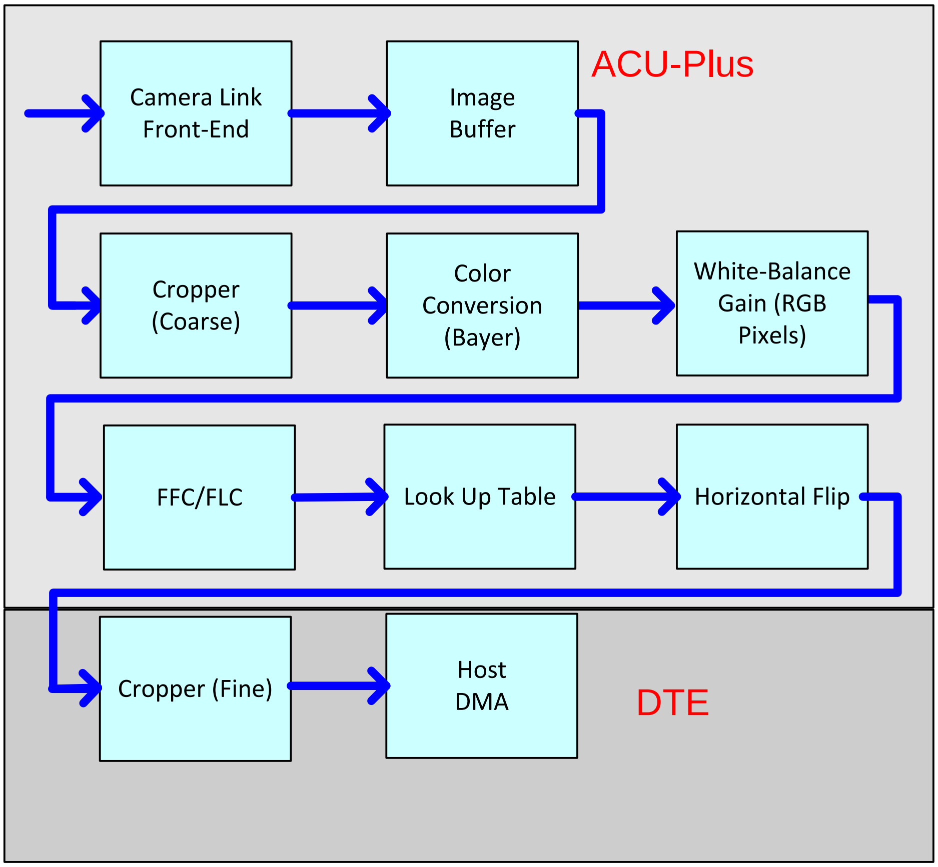


Figure 13: Xtium-CL MX4 Flow Diagram

- **Camera Link Front End:** Extracts the clock, LVAL, FVAL and data from the Camera Link ports based on the Camera Link configuration selected.
- **Image Buffer:** Stores the video data using the model of video frames.
- **Cropper (Coarse):** Horizontal cropper used when reading out from the memory.
- **Color Conversion:** When enabled for particular cameras, converts Bayer and Bi-Color video data into RGB data.
- **White Balance Gain:** Applies White Balance Gain to RGB data.
- **FFC/FLC:** Flat Field/Flat Line correction. Applies to Monochrome data only.
- **Lookup Tables:** Applies lookup table transformation to the data going to the host memory.
- **Horizontal Flip:** Performs the line data flip process.
- **Cropper (Fine):** Crops the resulting image when used, using a 4-byte resolution.
- **Host DMA:** Transfers the data from frame grabber into the host buffer memory. This module will also perform the vertical flip if enabled.

Acquisition Timing

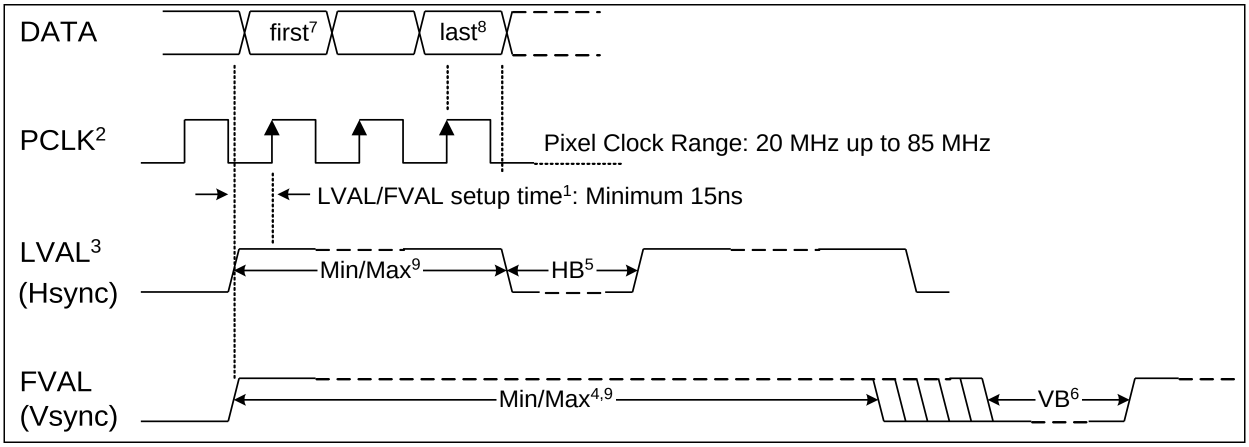


Figure 14: Acquisition Timing

▪ [1] The setup times for LVAL and FVAL are the same. Both must be high and stable before the rising edge of the Pixel Clock.	
▪ [2] Pixel Clock must always be present	
▪ [3] LVAL must be active high to acquire camera data	
▪ [4] Minimum of 1	
▪ [5] HB - Horizontal Blanking: Minimum: 1 clock cycle Maximum: no limits	▪ [6] VB - Vertical Blanking: Minimum: 1 line Maximum: no limits
▪ [7] First Active Pixel (unless otherwise specified in the CCA file – "Horizontal Back invalid = x" where 'x' defines the number of pixels to be skipped). ▪	
▪ [8] Last Active Pixel – defined in the CCA file under "Horizontal active = y" – where 'y' is the total number of active pixels per tap.	
▪ [9] Maximum Valid Data: ▪ 8-bits/pixel x 64k Pixels/line (LVAL) ▪ 16-bits/pixel x 32k Pixels/line (LVAL) ▪ 32-bits/pixel x 16k Pixels/line (LVAL) ▪ 16 Million lines (FVAL)	

Line Trigger Source Selection for Line scan Applications

Line scan imaging applications require some form of external event trigger to synchronize line scan camera exposures to the moving object. This synchronization signal is either an external trigger source (one exposure per trigger event) or a shaft encoder source composed of a single or dual phase signal (also known as a quadrature).

The Xtium-CL MX4 shaft encoder inputs provide additional functionality with pulse drop, pulse multiply, and pulse direction support.

The following table describes the line-trigger source types supported by the Xtium-CL MX4. Refer to the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00) for descriptions of the Sapera parameters.

Parameter Values Specific to the Xtium-CL MX4

PRM Value	Configuration & Input used	Input used as: External Line Trigger	Input used as: External Shaft Encoder
		if CORACQ_PRM_EXT_LINE_ TRIGGER_ENABLE = *true*	*if* CORACQ_PRM_SHAFT_ ENCODER_ENABLE =*true*
0	Dual – Camera #1 Dual – Camera #2 Full/80bit	From Shaft Encoder Phase A (default) From Shaft Encoder Phase B (default) From Shaft Encoder Phase A (default)	From Shaft Encoder Phase A (default) From Shaft Encoder Phase B (default) From Shaft Encoder Phase A & B (default)
1	Dual – Camera #1 Dual – Camera #2 Full/80bit	From Shaft Encoder Phase A	From Shaft Encoder Phase A
2	Dual – Camera #1 Dual – Camera #2 Full/80bit	From Shaft Encoder Phase B	From Shaft Encoder Phase B
3	Dual – Camera #1 Dual – Camera #2 Full/80bit	n/a	From Shaft Encoder Phase A & B
4		From Board Sync #1	n/a
5		From Board Sync #2	n/a

CVI/CCF File Parameters Used

- External Line Trigger Source = prm value
- External Line Trigger Enable = true/false
- Shaft Encoder Enable = true/false

Shaft Encoder Interface Timing

Dual Balanced Shaft Encoder RS-422 Inputs:

- Input Phase A: Connector J1/J4: Pin 3 (Phase A +) & Pin 2 (Phase A -)
- Input Phase B: Connector J1/J4: Pin 6 (Phase B+) & Pin 5 (Phase B-)
- See J1: External Signals Connector (Female DH60-27P) for complete connector signal details)

Web inspection systems with variable web speeds typically provide one or two synchronization signals from a web mounted encoder to coordinate trigger signals. These trigger signals are used by the acquisition line scan camera. The Xtium-CL MX4 supports single or dual phase shaft encoder signals. Dual encoder signals are typically 90 degrees out of phase relative to each other and provide greater web motion resolution.

Example using any Encoder Input with Pulse-drop Counter

When enabled, the triggered camera acquires one scan line for each shaft encoder pulse-edge. To optimize the web application, a second Sapera parameter defines the number of triggers to skip between valid acquisition triggers. The figure below depicts a system where a valid camera trigger is any pulse edge from either shaft encoder signal. After a trigger, the two following triggers are ignored (as defined by the Sapera pulse drop parameter).

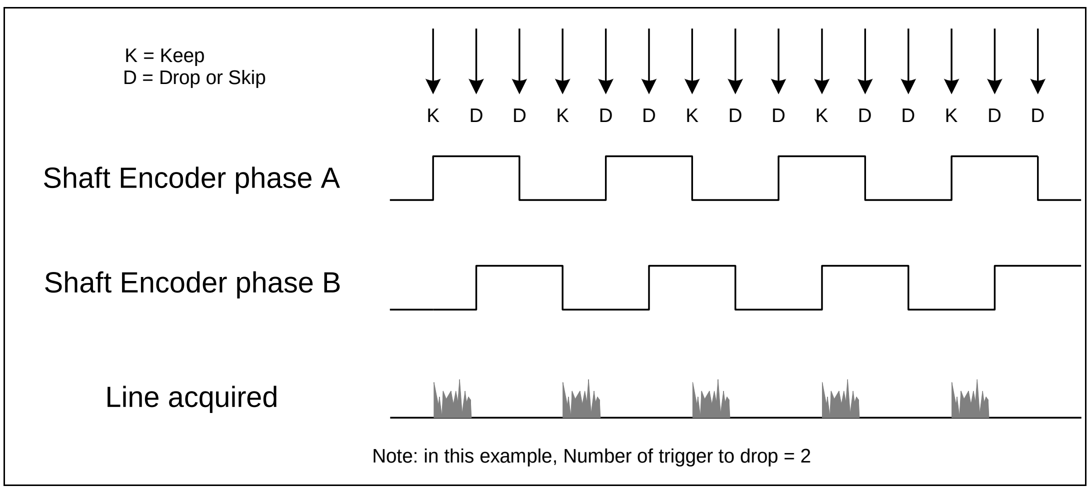


Figure 15: Encoder Input with Pulse-drop Counter

Example using Sequential Encoder Input

Support of a dual phase encoder should consider the direction of motion of one phase signal to the other. Such a case might exist where system vibrations and/or conveyor backlash can cause the encoder to briefly travel backwards. The acquisition device must in those cases count the reverse steps and subtract the forward steps such that only pulses after the reverse count reaches zero are considered. By using the event "Shaft Encoder Reverse Counter Overflow", an application can monitor an overflow of this counter.

Also, if a maximum line rate camera trigger source is a high jitter shaft encoder, the parameter CORACQ_PRM_LINE_TRIGGER_AUTO_DELAY can be used to automatically delay line triggers to avoid over-triggering a camera, and thus not miss a line. Note that some cameras integrate this feature. See also the event "Line Trigger Too Fast" that can be enabled when using the 'auto delay' feature.

The example figure below shows shaft encoder signals with high jitter. If the acquisition is triggered when phase B follows phase A, with jitter present phase B may precede phase A. Use of the *Shaft Encoder Direction* parameter will prevent false trigger conditions.

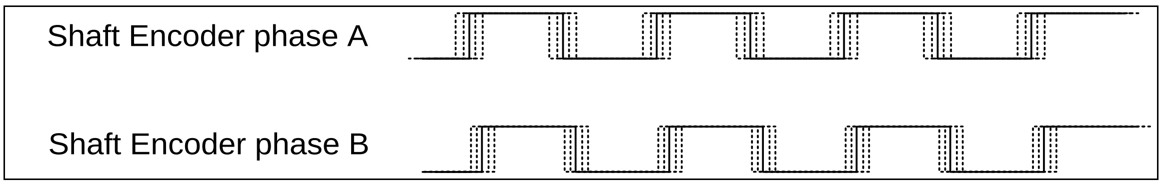


Figure 16: Using Shaft Encoder Direction Parameter

	Note: Modify camera file parameters easily with the Sapera CamExpert program.

CVI/CCF File Parameters Used

Shaft Encoder Enable = X, where:

- If X = 1, Shaft Encoder is enabled
- If X = 0, Shaft Encoder is disabled

Shaft Encoder Pulse Drop = X, where:

- X = number of trigger pulses ignored between valid triggers

Shaft Encoder Pulse Multiply = X, where:

- X = number of trigger pulses generated for each shaft encoder pulses

Shaft Encoder Pulse Drop/Multiply Order = X, where:

- If X = 1, the drop operation will be done first, followed by the multiplier operation
- If X = 0 or 2, the multiplier operation will be done first, followed by the drop operation

Shaft Encoder Direction = X, where:

- X = 0, Ignore direction
- X = 1, Forward steps are detected by pulse order A/B (forward motion)
- X = 2, Forward steps are detected by pulse order B/A (reverse motion)

Shaft Encoder Level = X, where:

- X = 1, TTL (Rev B Only)
- X = 2, RS-422

	Note: For information on camera configuration files, see the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

Virtual Frame Trigger for Line Scan Cameras

When using line scan cameras, a frame buffer is allocated in host system memory to store captured video lines. To control when a video line is stored as the first line in this "**virtual**" frame buffer, an external frame trigger signal is used.

For **fixed length** frames, the Sapera vertical cropping parameter controls the number of lines sequentially grabbed and stored in the virtual frame buffer.

For **variable length** frames, the External Frame Trigger (when a level or dual input type is selected) controls the number of lines sequentially grabbed up to the maximum of lines in the virtual frame buffer.

For both fixed and variable length frames, choosing an active low/high or dual input permits grabbing multiple consecutive images as long as the chosen signal is active. This action is also called "rolling over" to the next buffer. When choosing a single rising or falling edge, a single frame will be acquired, there is never any roll over.

External Frame Trigger Detection	Fixed Frame	Variable Frame
Active Low/High	Roll Over	Roll Over
Rising/Falling Edge	No Roll Over	No Roll Over
Dual Input Rising/Falling Edge	Roll Over	Roll Over

Virtual Frame Trigger Timing Diagrams

The following timing diagrams show the use of a virtual frame trigger to define when an image line is stored at the beginning of the virtual frame buffer. The virtual frame trigger signal (generated by some external event) connects to the Xtium-CL MX4 trigger input.

- Virtual frame trigger can be differential (RS-422) or single ended (TTL, 12V, 24V) industry standard, and be rising or falling edge active, active high or low, or double pulse rising or falling edge.
- Virtual frame trigger connects to the Xtium-CL MX4 via the External Trigger Input 1 & 2 inputs.
  - Trigger Input #1 on connector J1: pin 8
  - Trigger Input #2 on connector J1: pin 9
- The Sapera vertical cropping parameter specifies the number of lines captured (maximum size of virtual frame).

Synchronization Signals for a 10 Line Virtual Frame

The following timing diagram shows an example of grabbing 10 image lines from a line scan camera and the use of a virtual frame trigger to define when a video line is stored at the beginning of the virtual frame buffer.

In this example, virtual frame trigger control is configured for rising edge trigger.

- Camera control signals are active at all times. These continually trigger the camera acquisition in order to avoid corrupted video lines at the beginning of a virtual frame.
- The camera control signals are either timing controls on Xtium-CL MX4 shaft encoder inputs, or line triggers generated internally by the Xtium-CL MX4.

The following timing diagram shows the relationship between External Frame Trigger input, External Shaft Encoder input (one phase used with the second terminated), and camera control output to the camera.

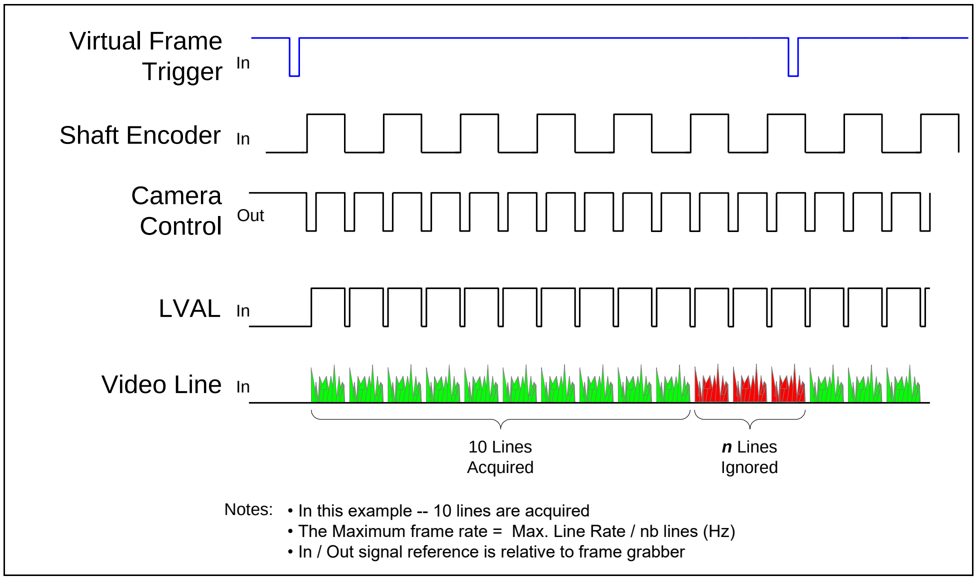


Figure 17: Synchronization Signals for a 10 Line Virtual Frame

Synchronization Signals for Fixed Frame Length Acquisition

A trigger event is only generated when a grab is active; when not grabbing no trigger events are generated. When a frame is complete, the frame grabber checks for the specified active trigger level and, if present, grabs the next frame; otherwise, it waits for the next detected active trigger level.

In the following diagrams:

"*T*" indicates a valid external trigger event (SapAcquisition::EventExternalTrigger).
"*Ignored*" is an ignored event (SapAcquisition::EventExternalTriggerIgnored).

such that

Ignored + *T* = total triggers received by frame grabber

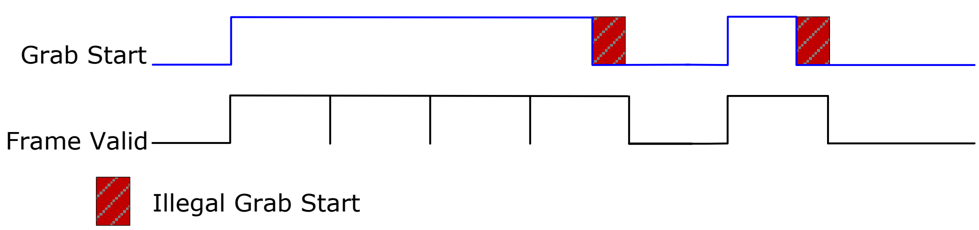


Figure 18: Line scan, Fixed Frame, No Trigger

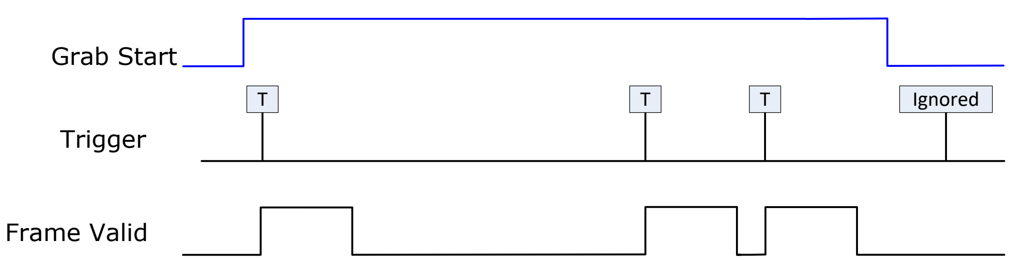


Figure 19: Line scan, Fixed Frame, Edge Trigger

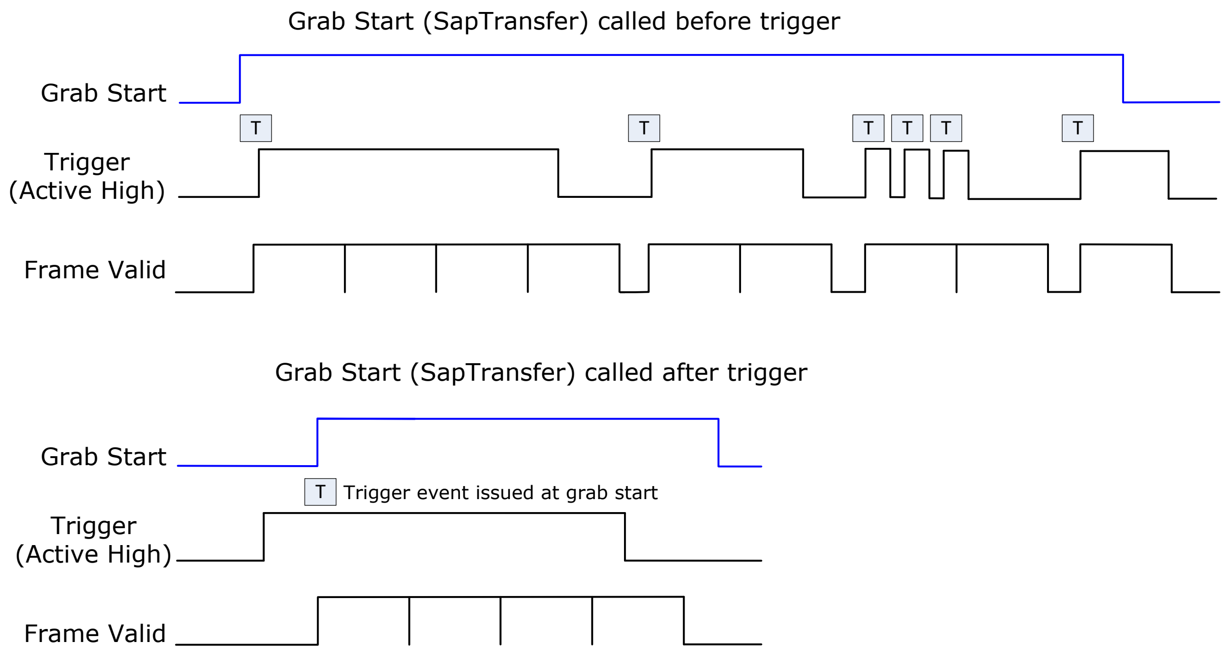


Figure 20: Line scan, Fixed Frame, Level Trigger (Roll-Over to Next Frame)

Synchronization Signals for Variable Frame Length Acquisition

For variable length frames, trigger ignored events are not issued (SapAcquisition::EventExternalTriggerIgnored); a valid trigger event always initiates either a frame start or frame end.

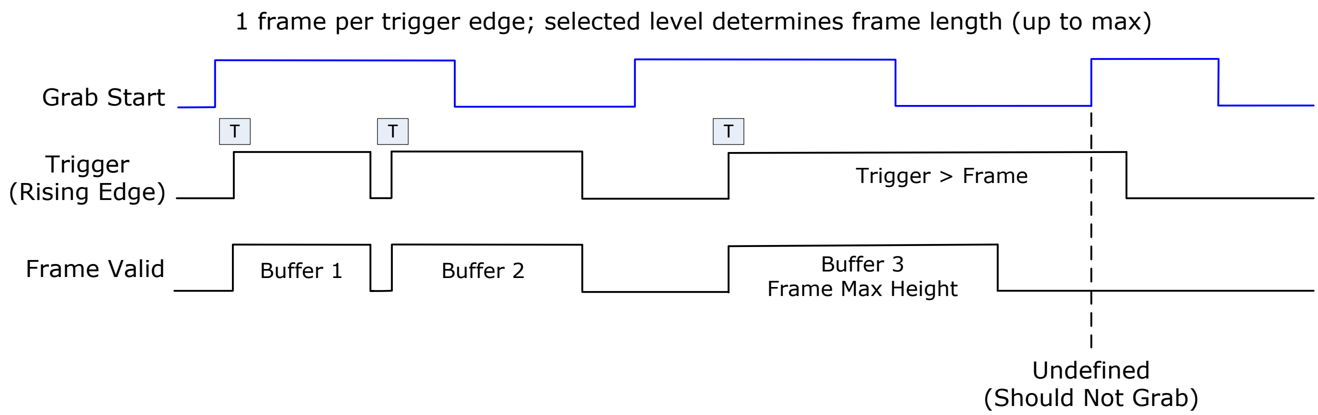


Figure 21: Line scan, Variable Frame, Edge Trigger (Active High determines Frame Length)

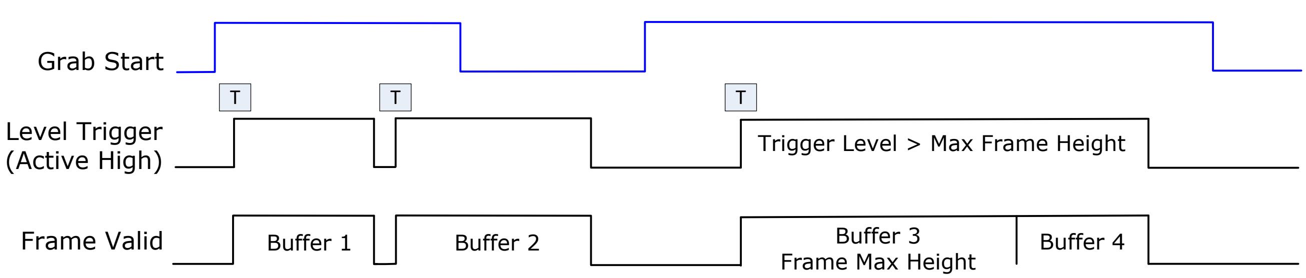


Figure 22: Line scan, Fixed Frame, Level Trigger (Roll-Over)

CVI File (VIC) Parameters Used

The VIC parameters listed below provide the control functionality for virtual frame trigger. Sapera applications load pre-configured CVI files or change VIC parameters during runtime.

ℹ	**Note:** Sapera camera file parameters are easily modified by using the CamExpert program.

External Frame Trigger Enable = X, where: (*with Virtual Frame Trigger enabled*)

- If X = 1, External Frame Trigger is enabled
- If X = 0, External Frame Trigger is disabled

External Frame Trigger Detection = Y, where:
If Y= 1, External Frame Trigger is active low

- If Y = 2, External Frame Trigger is active high
- If Y = 4, External Frame Trigger is active on rising edge
- If Y = 8, External Frame Trigger is active on falling edge
- If Y = 32, External Frame Trigger is dual-input rising edge
- If Y = 64, External Frame Trigger is dual-input falling edge

ℹ	**Note:**. For dual-input triggers, Trigger Input #1 signals the start of the frame trigger, Trigger Input #2 signals the end of the frame trigger.

External Frame Trigger Level = Z, where: (*with Virtual Frame Trigger signal type*)

- If Z = 1, External Frame Trigger is a TTL signal
- If Z = 2, External Frame Trigger is a differential signal (RS-422)
- If Z = 8, External Frame Trigger is a 24V signal
- If Z = 64, External Frame Trigger is a 12V signal

ℹ	**Note:** For information on camera configuration files, see the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

Sapera Acquisition Methods

Sapera acquisition methods define the control and timing of the camera and frame grabber board. Various methods are available, grouped as:

- Camera Trigger Methods (method 1 supported)
- Line Trigger Methods (method 1)
- Line Integration Methods (method 1 through 4 supported)
- Time Integration Methods (method 1, 3, 5, 6, 8)
- Strobe Methods (method 1, 3, 4 supported)

Refer to the Sapera LT Acquisition Parameters Reference manual (OC-SAPM-APR00) for detailed information concerning camera and acquisition control methods.

Trigger to Image Reliability

Trigger-to-image reliability incorporates all stages of image acquisition inside an integrated controller to increase reliability and simplify error recovery. The trigger-to-image reliability model brings together all the requirements for image acquisition to a central management unit. These include signals to control camera timing, on-board frame buffer memory to compensate for PCI bus latency, and comprehensive error notification. If the Xtium-CL MX4 detects a problem, the application can take appropriate action to return to normal operation.

The Xtium-CL MX4 is designed with a robust ACU (Acquisition and Control Unit). The ACU monitors in real-time, the acquisition state of the input plus the DTE (Data Transfer Engine) which transfers image data from on-board memory into PC memory. In general, these management processes are transparent to end-user applications. With the Xtium-CL MX4, applications ensure trigger-to-image reliability by monitoring events and controlling transfer methods as described below:

Supported Events and Transfer Methods

Listed below are the supported acquisition and transfer events. Event monitoring is a major component to the Trigger-to-Image Reliability framework.

Acquisition Events

Acquisition events pertain to the acquisition module and provide feedback on the image capture phase.

Event	Description
External Trigger (Used/Ignored)	Generated when the external trigger pin is asserted, which indicates the start of the acquisition process. There are two types of external trigger events: 'Used' or 'Ignored'. Following an external trigger, if the event generates a captured image, an External Trigger Used event will be generated (CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER). If there is no captured image, an External Trigger Ignored event will be generated (CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_IGNORED). An external trigger event is ignored if the event rate is higher than the possible frame rate of the camera.
Start of Frame	Event generated during acquisition, with the detection of the start of a video frame by the board acquisition hardware. The Sapera event value is CORACQ_VAL_EVENT_TYPE_START_OF_FRAME.
End of Frame	Event generated during acquisition, with the detection of the end of a video frame by the board acquisition hardware. The Sapera event value is CORACQ_VAL_EVENT_TYPE_END_OF_FRAME.
Data Overflow	The Data Overflow event indicates that there is not enough bandwidth for the acquired data transfer without loss. Data Overflow would occur with limitations of the acquisition module and should never occur. The Sapera event value is CORACQ_VAL_EVENT_TYPE_DATA_OVERFLOW.
Frame Valid	Event generated on detection of the start of a video frame by the board acquisition hardware. Acquisition does not need to be active; therefore, this event can verify a valid signal is connected. The Sapera event value is CORACQ_VAL_EVENT_TYPE_VERTICAL_SYNC.
Pixel Clock (Present/Absent)	Event generated on the transition from detecting or not detecting a pixel clock signal. The Sapera event values are CORACQ_VAL_EVENT_TYPE_NO_PIXEL_CLK and CORACQ_VAL_EVENT_TYPE_PIXEL_CLK.
Frame Lost	The Frame Lost event indicates that an acquired image failed to transfer to on-board memory. An example is if there are no free on-board buffers available for the new image. This may be the case if the image transfer from onboard buffers to host PC memory is not sustainable due to bus bandwidth issues or no host buffers are available to receive an image. The Sapera event value is CORACQ_VAL_EVENT_TYPE_FRAME_LOST.
External Line Trigger Too Slow	Event which indicates that the detected shaft encoder input tick rate is too slow for the device to take into account the specified shaft encoder multiplier value. The Sapera event value is CORACQ_VAL_EVENT_TYPE_EXT_LINE_TRIGGER_TOO_SLOW.
Line Trigger Too Fast	Event which indicates a previous line-trigger did not generate a complete video line from the camera. Note that due to jitter associated with using shaft encoders, the acquisition device can delay a line trigger if a previous line has not yet completed. This event is generated if a second line trigger comes in while the previous one is still pending. This event is generated once per virtual frame. The Sapera event value is CORACQ_VAL_EVENT_TYPE_LINE_TRIGGER_TOO_FAST.
Shaft Encoder Reverse Count Overflow	Event which indicates that the shaft encoder has travelled in the opposite direction expected and that the number of pulses encountered during that travel has exceeded the acquisition device counter. The acquisition device will thus not be able to skip the appropriate number of pulses when the expected direction is detected. The Sapera event value is CORACQ_VAL_EVENT_TYPE_SHAFT_ENCODER_REVERSE_COUNT_OVERFLOW.

Transfer Events

Transfer events are related to the transfer module and provide feedback on image transfer from onboard memory frame buffers to PC memory frame buffers.

Event	Description
Start of Frame	Start of Frame event generated when the first image pixel is transferred from on-board memory into PC memory. The Sapera event value is CORXFER_VAL_EVENT_TYPE_START_OF_FRAME.
End of Frame	End of Frame event generated when the last image pixel is transferred from on-board memory into PC memory. The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_FRAME.
End of Line	The End of Line event is generated after a video line is transferred to a PC buffer. The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_LINE.
End of N Lines	The End of N Lines event is generated after a set number of video lines are transferred to a PC buffer. The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_NLINES.
End of Transfer	End of Transfer event generated at the completion of the last image transfer from on-board memory into PC memory. Issue a stop command to the transfer module to complete a transfer (if transfers are already in progress). If a frame transfer of a fixed number of images is requested, the transfer module will stop transfer automatically. The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_TRANSFER.

Trigger Signal Validity

The ACU ignores external trigger signal noise with its programmable debounce control. Program the debounce parameter for the minimum pulse duration considered as a valid external trigger pulse. For more information see Note 1: General Inputs / External Trigger Inputs Specifications.

Supported Transfer Cycling Methods

The Xtium-CL MX4 supports the following transfer modes, which are either synchronous or asynchronous. Note that the Xtium does not make any use of the trash buffer. Images are accumulated in on-board memory in a FIFO type manner. On-board memory can get filled up if the rate at which the images are acquired is greater than the rate at which the DMA engine can write them to host buffer memory. On-board memory can also get filled-up if there are no more empty buffers available to transfer the on-board images.

When no memory is available for a new image to be stored in on-board memory, the image is discarded and a CORACQ_VAL_EVENT_TYPE_FRAME_LOST or trash buffer callback is generated. If a CORACQ_VAL_EVENT_TYPE_FRAME_LOST occurs when host buffers are available, it can indicate a problem with the MX4 bus bandwidth.

If image buffers are constructed using a trash buffer (SapBufferWithTrash using a transfer cycle mode with trash), when no host buffers are available and no memory is available for a new image to be stored in on-board memory, the SapXferCallBackInfo::IsTrash (C++) function or SaxXferNotifyEventsArgs.Trash (.NET) property returns true. If a trash callback function has been registered during construction of the SapTransfer object, it will be executed when a trash event occurs.

When stopping the image acquisition, the event CORXFER_VAL_EVENT_TYPE_END_OF_TRANSFER will occur once all images currently in the on-board memory are transferred to host buffer memory. Note that if the application does not provide enough empty buffers, the Xtium event will not occur and an acquisition abort will be required.

- CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_WITH_TRASH
  Before cycling to the next buffer in the list, the transfer device will check the next buffer's state. If its state is full, the transfer will keep the image in on-board memory until the next buffer's state changes to empty. If the on-board memory gets filled, trash callbacks will be generated.
- CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_NEXT_EMPTY_WITH_TRASH
  When starting an acquisition, the buffer list is put in an empty buffer queue list in the exact order they were added to the transfer. Whenever a user sets a buffer to empty, it is added to the empty buffer queue list, so that after cycling once through the original buffer list, the buffers acquired into will follow the order in which they are put empty by the user. So in this mode, the on-board images will be transferred to host buffer memory as long as there are buffers in the empty buffer queue list. If no buffers are available on the host and the on-board memory gets filled, trash callbacks will be generated.
- CORXFER_VAL_CYCLE_MODE_ASYNCHRONOUS
  The transfer device cycles through all buffers in the list without concern about the buffer state.

The following table describes the possible buffer states and resulting behavior:

Trash Buffer (cycling mode with trash)	**Xtium2 On-Board Memory State**	**Host Sapera Buffer State**	**Resulting Event**
NO	Empty buffer available (at least 1)	Empty buffer available (at least 1)	Normal acquisition events
NO	Empty buffer available (at least 1)	Full	Acquire into Xtium on-board memory
NO	Full	Empty buffer available (at least 1)	Frame Lost Event
NO	Full	Full	Frame Lost Event
YES	Empty buffer available (at least 1)	Empty buffer available (at least 1)	Normal acquisition events
YES	Empty buffer available (at least 1)	Full	Acquire into Xtium on-board memory
YES	Full	Empty buffer available (at least 1)	Frame Lost Event
YES	Full	Full	Trash Callback

- By default, the buffer state (empty or full) is automatically managed by Sapera LT; it can be managed manually by the user if necessary.

Output LUT Availability

The following table defines the supported output LUT (look up tables) for the Xtium-CL MX4. Note that unsupported modes are not listed.

Number of Digital Bits	Output Pixel Format	LUT Format	Notes*
8 8	MONO 8 MONO 16	8-in, 8-out 8-in, 16-out	8 bits in 8 LSBs of 16-bit
10	MONO 8	10-in, 8-out	
10	MONO 16	10-in, 16-out	10 bits in 10 LSBs of 16-bit
12	MONO 8	12-in, 8-out	8 MSB
12	MONO 16	12-in, 16-out	12 bits in 12 LSBs of 16-bit
8 x 3 (RGB)	RGB888	8-in, 8-out	
8 x 3 (RGB)	RGB8888	8-in, 8-out	
10 x 3 (RGB)	RGB888 RGB8888 RGB101010 RGB16161616	10-in, 8-out 10-in, 8-out 10-in, 10-out 10-in, 16-out	10 bits in 10 LSBs of 16-bit
12 x 3 (RGB)	RGB888 RGB8888 RGB101010 RGB16161616	12-in, 8-out 12-in, 8-out 12-in, 10-out 12-in, 16-out	12 bits in 12 LSBs of 16-bit

*When no LUTs are available or LUTs are disabled, the data is packed in the LSBs of the target destination.

Metadata: Theory of Operation

The following provides additional details on the Metadata implementation.

Metadata Data Structure

The Xtium-CL MX4 supports metadata at the end of each line when enabled through the parameter CORACQ_PRM_META_DATA. The metadata consists of 64 bytes. The content of the metadata represents a snapshot of the state of the frame grabber at the beginning of each LVAL received.

```
typedef struct
{
  ULONGLONG shaftEncoderCount;
  ULONGLONG lineCount;
  ULONGLONG lineTriggerCount;
  ULONGLONG timeStamp;
  ULONG frameCounter;
  UCHAR generalInputs;
  UCHAR generalOutputs;
  UCHAR biDirectionalIOs;
  UCHAR reserved[25];


} MX4_METADATA, *PMX4_METADATA;
```

- **shaftEncoderCount**: 64-bit counter of pulses received on the shaft encoder. This is a 'machine counter' that increments in one direction (forward) and decrements (reverse) in the opposite direction.
- **lineCount**: 64-bit counter of line valid (LVAL) received.
- **lineTriggerCount**: 64-bit counter of line triggers sent to the camera.
- **timeStamp**: 64-bit counter of the frame grabber on-board timestamp. See also CORACQ_PRM_TIME_STAMP_BASE and CORACQ_PRM_TIME_STAMP.
- **frameCounter**: 32-bit counter of frames received. This represents the frame number that the line belongs to.
- **generalInputs**: status of the general inputs (for example, Low, bit = 0 or High, bit = 1).
- **generalOutputs**: status of the general outputs (for example, Low, bit =0 or High, bit = 1).
- **biDirectionalIOs**: status of the bi-directional I/Os (for example, Low, bit = 0 or High, bit = 1).
- **reserved**: 25 bytes reserved for future usage.

For a demo application showing this feature, please contact Teledyne DALSA technical support.

Flat Field Correction: Theory of Operation

The following provides additional details on the Flat Field Correction and Flat Line Correction (FFC/FLC) implementation.

Flat Field Correction Lists

The Xtium-CL MX4 supports defining more than one Flat Field Correction (FFC) / Flat Line Correction (FLC) data sets. Using the Xfer parameter CORXFER_PRM_FLATFIELD_CYCLE_MODE, the user can decide to cycle automatically through the list of FFC/FLC sets by setting the parameter to CORXFER_VAL_FLATFIELD_CYCLE_MODE_AUTOMATIC, or select a specific FFC/FLC set from the list by setting the parameter to CORXFER_VAL_FLATFIELD_CYCLE_MODE_OFF and selecting the FFC/FLC index to use with the parameter CORACQ_PRM_FLAT_FIELD_SELECT.

While the cycling mode is set to off, users can upload new coefficients to an inactive FFC set even when grabbing. When cycling automatically, the FFC/FLC sets are selected in a round-robin fashion, changing at the beginning of every new frame.

The architecture of the Xtium-CL MX4 is such that the FFC/FLC data sets are independent of the host buffers. In automatic mode, the FFC/FLC sets are chosen in a round-robin fashion as images are acquired. So if using the Xfer cycling mode Synchrounous with Trash, it is recommended that the number of host buffers be a multiple of the number of FFC/FLC in the list in order to maintain the FFC/FLC relationship with the Host buffers.

- When the FFC/FLC cycle mode automatic is active, reset the acquisition module to start on the 1st FFC/FLC data set of the selected list as follows:
  - Disconnect/Reconnect the transfer (assuming 1st buffer is empty).
  - Selecting a set using the CORACQ_PRM_FLAT_FIELD_SET_SELECT parameter will choose the 1st FFC/FLC in the list of the selected set.

- When the FFC/FLC cycle mode automatic is active, start the acquisition module to start on a specific FFC/FLC of the selected list as follows:
  - While acquisition is stopped, by selecting an Xfer pair [ACQ, Buffer]. The index of the FFC/FLC will be selected based on the modulo of the number of FFC/FLC in the list with respect to the [ACQ, Buffer] index pair.

Flat Field Correction Sets

The concept of sets allows a user to define multiple lists of FFC/FLC correction data. The FFC/FLC API allows users to allocate and pre-program those FFC/FLC sets. When acquiring images, the board driver will cycle through the FFC/FLC list of the selected set. During that operation, users can upload new FFC/FLC data to non-active sets without any ill effects.

When changing the active set while grabbing, the new active set will be switched when the current cycling of the current list is completed.

Xtium-CL MX4 specific limitations

- Software driver permits the creation of up to 16 FFC/FLC sets.
- Software driver permits the use of up to 16 sets.
- When the FFC cycling mode is off, the concept of sets is not used. Whichever a FFC index is chosen using CORACQ_PRM_FLAT_FIELD_SELECT, it will be used independently of the set it belongs to.
- Upload of any FFC data is permitted at any time, even while grabbing. If an upload is done to an FFC index of the currently select set while grabbing, then the resulting acquired image will be undefined.
- When changing FFC cycling mode, the acquisition must be stopped.

Programming the sets

The following scheme is used to program FFC/FLC data within a set:

```
// select an active set
CorAcqSetPrm( hAcq, CORAQ_PRM_FLAT_FIELD_SET_SELECT, 0);

// Create 4 new FFC that will be part of the currently active set '0'
For( i = 0; i < 4; i++)
{
CorAcqNewFlatfield( hAcq, pFlatfieldNumber); // Will create FFC #1, #2, #3, #4
}

// select an active set
CorAcq  SetPrm( hAcq, CORAQ_PRM_FLAT_FIELD_SET_SELECT, 1);

// Create 4 new FFC that will be part of the currently active set '1'
For( i = 0; i < 4; i++)
{
CorAcqNewFlatfield( hAcq, pFlatfieldNumber); // Will create FFC #5, #6, #7, #8
}
```

Xtium-CL MX4 Supported Parameters

The tables below describe the Sapera capabilities supported by the Xtium-CL MX4. Unless specified, each capability applies to all configuration modes and all acquisition modes.

	The information here is subject to change. The application needs to verify capabilities. New board driver releases may change product specifications.

Sapera describes the Xtium-CL MX4 family as:

- **Board Server**: Xtium-CL_MX4_1
- **Acquisition Module**: *dependent on firmware used*

Camera Related Capabilities

Capability	Values
CORACQ_CAP_CONNECTOR_TYPE	CORACQ_VAL_CONNECTOR_TYPE_CAMLINK (0x2)
CORACQ_CAP_CONNECTOR_CAMLINK (Pin – 01, Pin – 02, Pin – 03, Pin - 04)	CORACQ_VAL_SIGNAL_NAME_NO_CONNECT (0x1) CORACQ_VAL_SIGNAL_NAME_PULSE0 (0x8) CORACQ_VAL_SIGNAL_NAME_PULSE1 (0x10) CORACQ_VAL_SIGNAL_NAME_GND (0x4000) CORACQ_VAL_SIGNAL_NAME_EXT_TRIGGER_1 (0x200) CORACQ_VAL_SIGNAL_NAME_EXT_TRIGGER_2 (0x200000) CORACQ_VAL_SIGNAL_NAME_SHAFT_ENCODER_PHASE_A (0x40000) CORACQ_VAL_SIGNAL_NAME_SHAFT_ENCODER_PHASE B (0x80000) CORACQ_VAL_SIGNAL_NAME_EXT_LINE_TRIGGER_1 (0x400) CORACQ_VAL_SIGNAL_NAME_EXT_LINE_TRIGGER_2 (0x100000)

Camera Related Parameters

Parameter		Values
CORACQ_PRM_CHANNEL		CORACQ_VAL_CHANNEL_SINGLE (0x1) CORACQ_VAL_CHANNEL_DUAL (0x2)
CORACQ_PRM_FRAME		CORACQ_VAL_FRAME_PROGRESSIVE (0x2)
CORACQ_PRM_INTERFACE		CORACQ_VAL_INTERFACE_DIGITAL (0x2)
CORACQ_PRM_SCAN		CORACQ_VAL_SCAN_AREA (0x1) CORACQ_VAL_SCAN_LINE (0x2)
CORACQ_PRM_SIGNAL		CORACQ_VAL_SIGNAL_DIFFERENTIAL (0x2)
CORACQ_PRM_VIDEO	*Base/Full Mono* *10T8B Mono /* *8T10B Mono*	CORACQ_VAL_VIDEO_MONO (0x1) CORACQ_VAL_VIDEO_BAYER (0x10)
	Base/Medium Color RGB *Full Packed RGB* *80B Packed RGB*	CORACQ_VAL_VIDEO_RGB (0x8)
	Base/Full Bayer *10T8B Bayer* *8T10B Bayer*	CORACQ_VAL_VIDEO_BAYER (0x10)
	80B Packed Bi-Color	CORACQ_VAL_VIDEO_BICOLOR (0x20)
	Full Packed RGBY	CORACQ_VAL_VIDEO_RGBY (0x40)
CORACQ_PRM_PIXEL_DEPTH	*Base/Full mono*	8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO8 8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO16 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO8 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO16 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO8 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO16 14 bits, # LUT = 0, LUT format = CORDATA_FORMAT_MONO16 16 bits, # LUT = 0, LUT format = CORDATA_FORMAT_MONO16
	10T8B Mono	8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO8 8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO16
	8T10B Mono	10 bits, # LUT = 1, LUT format = CORDATA_FORMATMONO8 10 bits, # LUT = 1, LUT format = CORDATA_FORMATMONO16
	Base/Medium Color RGB *Base/Full Bayer*	8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI10 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI16 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI10 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI16
	Full Packed RGB *80B Packed Bi-Color* *10T8B Bayer*	8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8
	80B Packed RGB	8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI10 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI16
	8T10B Bayer	8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI10 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI16
	Full Packed RGBY	8 bits, # LUT = 0, LUT format = CORDATA_FORMAT_COLORNI8
CORACQ_PRM_VIDEO_STD		CORACQ_VAL_VIDEO_STD_NON_STD (0x1)
CORACQ_PRM_FIELD_ORDER		CORACQ_VAL_FIELD_ORDER_NEXT_FIELD (0x4)

CORACQ_PRM_HACTIVE	Base/Full Mono Base/Full Bayer	min = 4 pixel, max = 65536 pixel, step = 1 pixel
	10T8B Mono 10T8B Bayer	min = 4 pixel, max = 6553 pixel, step = 1 pixel
	8T10B Mono 8T10B Bayer	min = 4 pixel, max = 4096 pixel, step = 1 pixel
	Base/Medium Color RGB Full Packed RGB Full Packed RGBY	min = 4 pixel, max = 16384 pixel, step = 1 pixel
	80B Packed RGB	min = 4 pixel, max = 21845 pixel, step = 1 pixel
	80B Packed Bi-Color	min = 4 pixel, max = 32768 pixel, step = 1 pixel
CORACQ_PRM_HSYNC		min = 1 pixel max = 4294967295 pixel step = 1 pixel
CORACQ_PRM_VACTIVE		min = 1 line max = 16777215 line step = 1 line
CORACQ_PRM_VSYNC		min = 0 line max = 4294967295 line step = 1 line
CORACQ_PRM_HFRONT_INVALID		min = 0 pixel max = 65535 pixel step = 1 pixel
CORACQ_PRM_HBACK_INVALID		min = 0 pixel max = 65535 pixel step = 1 pixel
CORACQ_PRM_VFRONT_INVALID		min = 0 line max = 16777215 line step = 1 line
CORACQ_PRM_VBACK_INVALID		min = 0 line max = 16777215 line step = 1 line
CORACQ_PRM_PIXEL_CLK_SRC		CORACQ_VAL_PIXEL_CLK_SRC_EXT (0x2)
CORACQ_PRM_PIXEL_CLK_EXT		min = 20000000 Hz max = 85000000 Hz step = 1 Hz
CORACQ_PRM_SYNC		CORACQ_VAL_SYNC_SEP_SYNC (0x4)
CORACQ_PRM_HSYNC_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1)
CORACQ_PRM_VSYNC_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1)
CORACQ_PRM_TIME_INTEGRATE_METHOD		CORACQ_VAL_TIME_INTEGRATE_METHOD_1 (0x1) CORACQ_VAL_TIME_INTEGRATE_METHOD_3 (0x4) CORACQ_VAL_TIME_INTEGRATE_METHOD_5 (0x10) CORACQ_VAL_TIME_INTEGRATE_METHOD_6 (0x20) CORACQ_VAL_TIME_INTEGRATE_METHOD_8 (0x80)
CORACQ_PRM_CAM_TRIGGER_METHOD		CORACQ_VAL_CAM_TRIGGER_METHOD_1 (0x1)
CORACQ_PRM_CAM_TRIGGER_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_CAM_TRIGGER_DURATION		min = 1 µs max = 85899345 µs step = 1 µs
CORACQ_PRM_CAM_NAME	Base/Full Mono	Default Area Scan 1 tap Mono
	10T8B Mono	Default Area Scan 10 taps Parallel Mono
	8T10B Mono	Default Area Scan 8 taps Parallel Mono
	Base/Medium Color RGB	Default Area Scan 1 tap Color
	Base/Full Bayer	Default Bayer Area Scan 1 tap Color
	Full Packed RGB	Default Area Scan Full Packed RGB
	80B Packed RGB	Default Area Scan 80-bit Packed RGB
	80B Packed Bi-Color	Default Area Scan 80-bit Packed Bi-Color
	10T8B Bayer	Default Bayer Area Scan 10 taps Parallel Color
	8T10B Bayer	Default Bayer Area Scan 8 taps Parallel Color
	Full Packed RGBY	Default Line Scan Full Packed RGBY
CORACQ_PRM_LINE_INTEGRATE_METHOD		CORACQ_VAL_LINE_INTEGRATE_METHOD_1 (0x1) CORACQ_VAL_LINE_INTEGRATE_METHOD_3 (0x4) CORACQ_VAL_LINE_INTEGRATE_METHOD_4 (0x8)
CORACQ_PRM_LINE_TRIGGER_METHOD		CORACQ_VAL_LINE_TRIGGER_METHOD_1 (0x1)
CORACQ_PRM_LINE_TRIGGER_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)

CORACQ_PRM_LINE_TRIGGER_DELAY		min = 0 pixel max = 85899345 pixel step = 1 pixel
CORACQ_PRM_LINE_TRIGGER_DURATION		min = 0 pixel max = 85899345 pixel step = 1 pixel
CORACQ_PRM_TAPS	*Base/Full Mono* *Base/Full Bayer*	min = 1 tap, max = 9 taps, step = 1 tap
	10T8B Mono *10T8B Bayer*	min = 10 taps, max = 10 taps, step = 1 tap
	8T10B Mono *8T10B Bayer*	min = 8 taps, max = 8 taps, step = 1 tap
	Base/Medium Color RGB	min = 1 tap, max = 2 taps, step = 1 tap
	Full Packed RGB *Full Packed RGBY* *80B Packed RGB* *80B Packed Bi-Color*	min = 1 tap, max = 1 tap, step = 1 tap
CORACQ_PRM_TAP_OUTPUT	Base/Full Mono Base/Full Bayer	CORACQ_VAL_TAP_OUTPUT_ALTERNATE (0x1) CORACQ_VAL_TAP_OUTPUT_SEGMENTED (0x2) CORACQ_VAL_TAP_OUTPUT_PARALLEL (0x4)
	10T8B Mono 10T8B Bayer	CORACQ_VAL_TAP_OUTPUT_SEGMENTED (0x2) CORACQ_VAL_TAP_OUTPUT_PARALLEL (0x4)
	Full Packed RGB Full Packed RGBY 8T10B Mono 80B Packed RGB 80B Packed Bi-Color 8T10B Bayer	CORACQ_VAL_TAP_OUTPUT_PARALLEL (0x4)
	Base Medium Color RGB	CORACQ_VAL_TAP_OUTPUT_SEGMENTED (0x2)
	Medium Color RGB	CORACQ_VAL_TAP_OUTPUT_ALTERNATE (0x1) CORACQ_VAL_TAP_OUTPUT_SEGMENTED (0x2)
CORACQ_PRM_TAP_1_DIRECTION		CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_2_DIRECTION		CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_3_DIRECTION		CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_4_DIRECTION		CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_5_DIRECTION		CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_6_DIRECTION		CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)

CORACQ_PRM_TAP_7_DIRECTION	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_8_DIRECTION	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_PIXEL_CLK_DETECTION	CORACQ_VAL_RISING_EDGE (0x4)
CORACQ_PRM_CHANNELS_ORDER	CORACQ_VAL_CHANNELS_ORDER_NORMAL (0x1) CORACQ_VAL_CHANNELS_ORDER_REVERSE (0x2)
CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MIN	1 Hz
CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MAX	10000000 Hz
CORACQ_PRM_CAM_TIME_INTEGRATE_DURATION_MIN	1 µs
CORACQ_PRM_CAM_TIME_INTEGRATE_DURATION_MAX	85899345 µs
CORACQ_PRM_TIME_INTEGRATE_PULSE1_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_TIME_INTEGRATE_PULSE1_DELAY	min = 0 µs max = 85899345 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_PULSE1_DURATION	min = 1 µs max = 85899345 µs step = 1 µs
CORACQ_PRM_CAM_IO_CONTROL (*)	All 4 CCs can be driven with one of the following signals: Logic High Logic Low External Trigger #1 (redirect from physical input signal) External Trigger #2 (redirect from physical input signal) Shaft Encoder Phase A (redirect from physical input signal) Shaft Encoder Phase B (redirect from physical input signal) External Line Trigger #1(redirect from physical input signal) External Line Trigger #2(redirect from physical input signal)
CORACQ_PRM_TIME_INTEGRATE_PULSE0_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_TIME_INTEGRATE_PULSE0_DELAY	min = 0 µs max = 85899345 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_PULSE0_DURATION	min = 1 µs max = 85899345 µs step = 1 µs
CORACQ_PRM_LINE_INTEGRATE_PULSE1_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_LINE_INTEGRATE_PULSE1_DELAY	min = 0 pixel max = 85899345 pixel step = 1 pixel
CORACQ_PRM_LINE_INTEGRATE_PULSE1_DURATION	min = 1 pixel max = 85899345 pixel step = 1 pixel
CORACQ_PRM_LINE_INTEGRATE_PULSE0_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_LINE_INTEGRATE_PULSE0_DELAY	min = 0 pixel max = 85899345 pixel step = 1 pixel
CORACQ_PRM_LINE_INTEGRATE_PULSE0_DURATION	min = 1 pixel max = 85899345 pixel step = 1 pixel

CORACQ_PRM_CAMLINK_CONFIGURATION	Base Mono Base Bayer	CORACQ_VAL_CAMLINK_CONFIGURATION_BASE (0x1)
	Full Mono Full Bayer	CORACQ_VAL_CAMLINK_CONFIGURATION_BASE (0x1) CORACQ_VAL_CAMLINK_CONFIGURATION_MEDIUM (0x2) CORACQ_VAL_CAMLINK_CONFIGURATION_FULL (0x4)
	10T8B Mono 10T8B Bayer	CORACQ_VAL_CAMLINK_CONFIGURATION_10TAPS_FORMAT2 (0x40)
	8T10B Mono 8T10B Bayer	CORACQ_VAL_CAMLINK_CONFIGURATION_8TAPS_10BITS (0x80)
	Base Color RGB	CORACQ_VAL_CAMLINK_CONFIGURATION_BASE (0x1)
	Medium Color RGB	CORACQ_VAL_CAMLINK_CONFIGURATION_BASE (0x1) CORACQ_VAL_CAMLINK_CONFIGURATION_MEDIUM (0x2)
	Full Packed RGB Full Packed RGBY	CORACQ_VAL_CAMLINK_CONFIGURATION_FULL_PACKED (0x100) CORACQ_VAL_CAMLINK_CONFIGURATION_FLAG_BGR (0x80000000)
	80B Packed RGB	CORACQ_VAL_CAMLINK_CONFIGURATION_80BITS_PACKED (0x200) CORACQ_VAL_CAMLINK_CONFIGURATION_FLAG_BGR (0x80000000)
	80B Packed Bi-Color	CORACQ_VAL_CAMLINK_CONFIGURATION_80BITS_PACKED (0x200)
CORACQ_PRM_DATA_VALID_ENABLE	Base/Full Mono Base/Medium Color RGB Full Packed RGB Full Packed RGBY	TRUE FALSE
	10T8B Mono 8T10B Mono 80B Packed RGB 80B Packed Bi-Color 10T8B Bayer 8T10B Bayer	Not available
CORACQ_PRM_DATA_VALID_POLARITY		CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_TAP_9_DIRECTION	*Full Mono* *10T8B Mono* *10T8B Bayer*	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_10_DIRECTION	*10T8B Mono* *10T8B Bayer*	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_RL (0x2) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TIMESLOT		CORACQ_VAL_TIMESLOT_1 (0x1)
CORACQ_PRM_COLOR_ALIGNMENT	Base/Full Bayer 10T8B Bayer 8T10B Bayer	CORACQ_VAL_COLOR_ALIGNMENT_GB_RG (0x1) CORACQ_VAL_COLOR_ALIGNMENT_BG_GR (0x2) CORACQ_VAL_COLOR_ALIGNMENT_RG_GB (0x4) CORACQ_VAL_COLOR_ALIGNMENT_GR_BG (0x8)
	80B Packed Bi-Color	CORACQ_VAL_COLOR_ALIGNMENT_RGBG (0x10) CORACQ_VAL_COLOR_ALIGNMENT_BGRG (0x20)
CORACQ_PRM_CAM_CONTROL_DURING_READOUT		CORACQ_VAL_CAM_CONTROL_DURING_READOUT_INVALID (0x0) CORACQ_VAL_CAM_CONTROL_DURING_READOUT_VALID (0x1) CORACQ_VAL_CAM_CONTROL_DURING_READOUT_IGNORE (0x2)

VIC Related Parameters

Parameter		Values
CORACQ_PRM_CAMSEL	Base/Full Mono 10T8B Mono 8T10B Mono	CAMSEL_MONO = from 0 to 0
	Full Packed RGB Full Packed RGBY Base/Full Bayer 80B Packed Bi-Color 10T8B Bayer 8T10B Bayer Base/Medium Color RGB 80B Packed RGB	CAMSEL_RGB = from 0 to 0
CORACQ_PRM_CROP_LEFT	Base/Full Mono	min = 0 pixel, max = 65512 pixel, step = 2 pixel
	10T8B Mono	min = 0 pixel, max = 65506 pixel, step = 4 pixel
	Base/Full Bayer	min = 0 pixel, max = 65512 pixel, step = 1 pixel
	10T8B Bayer	min = 0 pixel, max = 65512 pixel, step = 1 pixel
	8T10B Mono	min = 0 pixel, max = 32744 pixel, step = 2 pixel
	8T10B Bayer	min = 0 pixel, max = 32744 pixel, step = 4 pixel
	Base/Medium Color RGB Full Packed RGB Full Packed RGBY	min = 0 pixel, max = 16380 pixel, step = 1 pixel
	80B Packed RGB	min = 0 pixel, max = 16380 pixel, step = 1 pixel
	80B Packed Bi-Color	min = 0 pixel, max = 32764 pixel, step = 1 pixel
CORACQ_PRM_CROP_TOP		min = 0 line max = 16777215 line step = 1 line
CORACQ_PRM_CROP_WIDTH	Base/Full Mono	min = 24 pixel, max = 65536 pixel, step = =2 pixel
	10T8B Mono	min = 24 pixel, max = 65530 pixel, step = =4 pixel
	Base/Full Bayer	min = 24 pixel, max = 65536 pixel, step = 1 pixel
	10T8B Bayer	min = 24 pixel, max = 65536 pixel, step = 1 pixel
	8T10B Mono	min = 24 pixel, max = 32768 pixel, step = 2 pixel
	8T10B Bayer	min = 24 pixel, max = 32768 pixel, step = 1 pixel
	Base/Medium Color RGB Full Packed RGB Full Packed RGBY	min = 4 pixel, max = 16384 pixel, step = 1 pixel
	80B Packed RGB	min = 4 pixel, max = 16384 pixel, step = 1 pixel
	80B Packed Bi-Color	min = 4 pixel, max = 32768 pixel, step = 1 pixel
CORACQ_PRM_CROP_HEIGHT		min = 1 line max = 16777215 line step = 1 line
CORACQ_PRM_DECIMATE_METHOD		CORACQ_VAL_DECIMATE_DISABLE (0x1)
CORACQ_PRM_LUT_ENABLE	Full Packed RGBY	Not Available
	All other modules	TRUE FALSE
CORACQ_PRM_LUT_NUMBER		Default = 0
CORACQ_PRM_STROBE_ENABLE		TRUE FALSE
CORACQ_PRM_STROBE_METHOD		CORACQ_VAL_STROBE_METHOD_1 (0x1) CORACQ_VAL_STROBE_METHOD_3 (0x4) CORACQ_VAL_STROBE_METHOD_4 (0x8)
CORACQ_PRM_STROBE_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_STROBE_DURATION		min = 1 µs max = 85899345 µs step = 1 µs
CORACQ_PRM_STROBE_DELAY		min = 0 µs max = 85899345 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_ENABLE		TRUE FALSE

CORACQ_PRM_TIME_INTEGRATE_DURATION		min = 1 µs max = 85899345 µs step = 1 µs
CORACQ_PRM_CAM_TRIGGER_ENABLE		TRUE FALSE
CORACQ_PRM_OUTPUT_FORMAT	*Base/Full Mono* *10T8B / 8T10B*	CORACQ_VAL_OUTPUT_FORMAT_MONO8 CORACQ_VAL_OUTPUT_FORMAT_MONO16 CORACQ_VAL_OUTPUT_FORMAT_MONO8P2 CORACQ_VAL_OUTPUT_FORMAT_MONO8P3 CORACQ_VAL_OUTPUT_FORMAT_MONO8P4
	Base/Medium Color RGB	CORACQ_VAL_OUTPUT_FORMAT_RGB8888 CORACQ_VAL_OUTPUT_FORMAT_RGB888 CORACQ_VAL_OUTPUT_FORMAT_RGB101010 CORACQ_VAL_OUTPUT_FORMAT_RGB16161616
	Base/Full Bayer	CORACQ_VAL_OUTPUT_FORMAT_RGB8888 CORACQ_VAL_OUTPUT_FORMAT_RGB888 CORACQ_VAL_OUTPUT_FORMAT_RGB101010 CORACQ_VAL_OUTPUT_FORMAT_RGB16161616 CORACQ_VAL_OUTPUT_FORMAT_MONO8 CORACQ_VAL_OUTPUT_FORMAT_MONO16
	Full Packed RGB	CORACQ_VAL_OUTPUT_FORMAT_RGB8888 CORACQ_VAL_OUTPUT_FORMAT_RGB888
	Full Packed RGBY	CORACQ_VAL_OUTPUT_FORMAT_RGB888_MONO8
	80B Packed RGB	CORACQ_VAL_OUTPUT_FORMAT_RGB8888 CORACQ_VAL_OUTPUT_FORMAT_RGB888 CORACQ_VAL_OUTPUT_FORMAT_RGB101010 CORACQ_VAL_OUTPUT_FORMAT_RGB16161616
	80B Packed Bi-Color	CORACQ_VAL_OUTPUT_FORMAT_RGB8888 CORACQ_VAL_OUTPUT_FORMAT_RGB888 CORACQ_VAL_OUTPUT_FORMAT_BICOLOR88
	10T8B Bayer	CORACQ_VAL_OUTPUT_FORMAT_RGB8888 CORACQ_VAL_OUTPUT_FORMAT_RGB888 CORACQ_VAL_OUTPUT_FORMAT_MONO8
	8T10B Bayer	CORACQ_VAL_OUTPUT_FORMAT_RGB8888 CORACQ_VAL_OUTPUT_FORMAT_RGB888 CORACQ_VAL_OUTPUT_FORMAT_RGB101010 CORACQ_VAL_OUTPUT_FORMAT_RGB16161616 CORACQ_VAL_OUTPUT_FORMAT_MONO16
CORACQ_PRM_EXT_TRIGGER_ENABLE		CORACQ_VAL_EXT_TRIGGER_OFF (0x1) CORACQ_VAL_EXT_TRIGGER_ON (0x8)
CORACQ_PRM_VIC_NAME	Base/Full Mono 10T8B Mono 8T10B Mono Base/Medium Color RGB Base/Full Bayer Full Packed RGB 80B Packed RGB 80B Packed Bi-Color 10T8B Bayer 8T10B Bayer Full Packed RGBY	Default Area Scan 1 tap Mono Default Area Scan 10 taps Parallel Mono Default Area Scan 8 taps Parallel Mono Default Area Scan 1 tap Color Default Bayer Area Scan 1 tap Color Default Area Scan Full Packed RGB Default Area Scan 80-bit Packed RGB Default Area Scan 80-bit Packed Bi-Color Default Bayer Area Scan 10 taps Parallel Color Default Bayer Area Scan 8 taps Parallel Color Default Line Scan Full Packed RGBY
CORACQ_PRM_LUT_MAX	Full Packed RGBY	0
	All other modules	1
CORACQ_PRM_EXT_TRIGGER_DETECTION		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2) CORACQ_VAL_RISING_EDGE (0x4) CORACQ_VAL_FALLING_EDGE (0x8)
CORACQ_PRM_LUT_FORMAT	*Base/Full mono/10T8B*	Default = CORDATA_FORMAT_MONO8
	8T10B	Default = CORDATA_FORMAT_MONO16
	Base/Medium Color RGB	Default = CORDATA_FORMAT_COLORNI8
	Base/Full Bayer	Default = CORDATA_FORMAT_COLORNI8
	Full Packed RGB *80B Packed RGB* *80B Packed Bi-Color*	Default = CORDATA_FORMAT_COLORNI8
	10T8B Bayer	Default = CORDATA_FORMAT_COLORNI8
	8T10B Bayer	Default = CORDATA_FORMAT_COLORNI10
CORACQ_PRM_VSYNC_REF		CORACQ_VAL_SYNC_REF_END (0x2)
CORACQ_PRM_HSYNC_REF		CORACQ_VAL_SYNC_REF_END (0x2)
CORACQ_PRM_LINE_INTEGRATE_ENABLE		TRUE FALSE

CORACQ_PRM_LINE_INTEGRATE_DURATION	min = 1 pixel max = 85899345 pixel step = 1 pixel
CORACQ_PRM_LINE_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_EXT_FRAME_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_EXT_FRAME_TRIGGER_DETECTION	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2) CORACQ_VAL_RISING_EDGE (0x4) CORACQ_VAL_FALLING_EDGE (0x8) CORACQ_VAL_DOUBLE_PULSE_RISING_EDGE (0x20) CORACQ_VAL_DOUBLE_PULSE_FALLING_EDGE (0x40) CORACQ_VAL_DOUBLE_PULSE_RISING_EDGE_ORDER_REVERSE (0x80) CORACQ_VAL_DOUBLE_PULSE_FALLING_EDGE_ORDER_REVERSE(0x100)
CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_EXT_LINE_TRIGGER_DETECTION	CORACQ_VAL_RISING_EDGE (0x4) CORACQ_VAL_FALLING_EDGE (0x8)
CORACQ_PRM_SNAP_COUNT	Not available
CORACQ_PRM_INT_LINE_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_INT_LINE_TRIGGER_FREQ	Default = 5000 Hz When reading back this parameter, the value returned will be what the frame grabber is set to, which may not be exactly what was programmed due to the frame grabber parameter's resolution.
CORACQ_PRM_BIT_ORDERING	CORACQ_VAL_BIT_ORDERING_STD (0x1)
CORACQ_PRM_EXT_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) CORACQ_VAL_LEVEL_422 (0x2) CORACQ_VAL_LEVEL_12VOLTS (0x040) CORACQ_VAL_LEVEL_24VOLTS (0x8)
CORACQ_PRM_STROBE_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1)
CORACQ_PRM_EXT_FRAME_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) CORACQ_VAL_LEVEL_422 (0x2) CORACQ_VAL_LEVEL_12VOLTS (0x040) CORACQ_VAL_LEVEL_24VOLTS (0x8)
CORACQ_PRM_EXT_LINE_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) : Rev B Only CORACQ_VAL_LEVEL_422 (0x2)
CORACQ_PRM_INT_LINE_TRIGGER_FREQ_MIN	8 Hz
CORACQ_PRM_INT_LINE_TRIGGER_FREQ_MAX	500000 Hz
CORACQ_PRM_MASTER_MODE	Not available
CORACQ_PRM_SHAFT_ENCODER_DROP	min = 0 tick max = 254 tick step = 1 tick
CORACQ_PRM_SHAFT_ENCODER_ENABLE	TRUE FALSE
CORACQ_PRM_EXT_TRIGGER_FRAME_COUNT	min = 1 frame max = 262142 frames step = 1 frame Note: Infinite not supported
CORACQ_PRM_INT_FRAME_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_INT_FRAME_TRIGGER_FREQ	min = 1 milli-Hz max = 1000000000 milli-Hz step = 1 milli-Hz
CORACQ_PRM_FRAME_LENGTH	CORACQ_VAL_FRAME_LENGTH_FIX (0x1) CORACQ_VAL_FRAME_LENGTH_VARIABLE (0x2)
CORACQ_PRM_FLIP — Full Packed RGBY	Not Available
CORACQ_PRM_FLIP — All other modules	CORACQ_VAL_FLIP_OFF (0x00) CORACQ_VAL_FLIP_HORZ (0x01)
CORACQ_PRM_EXT_TRIGGER_DURATION	min = 0 µs max = 255 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_DELAY	min = 0 µs max = 85899345 µs step = 1 µs

CORACQ_PRM_CAM_RESET_DELAY		min = 0 µs max = 0 µs step = 1 µs
CORACQ_PRM_CAM_TRIGGER_DELAY		min = 0 µs max = 85899345 µs step = 1 µs
CORACQ_PRM_SHAFT_ENCODER_LEVEL		CORACQ_VAL_LEVEL_TTL (0x1) : Rev B Only CORACQ_VAL_LEVEL_422 (0x2)
CORACQ_PRM_LUT_NENTRIES	8-bit/pixel component 10-bit/pixel component 12-bit/pixel component 14/16-bit/pixel component	256 entries 1024 entries 4096 entries 0 entries
CORACQ_PRM_EXT_FRAME_TRIGGER_SOURCE (*)		min = 0 max = 5 step = 1
CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE (*)		min = 0 max = 5 step = 1
CORACQ_PRM_EXT_TRIGGER_SOURCE (*)		min = 0 max = 5 step = 1
CORACQ_PRM_SHAFT_ENCODER_MULTIPLY		min = 1 max = 32 step = (2^N)
CORACQ_PRM_EXT_TRIGGER_DELAY		min = 0 max = 16777215 step = 1
CORACQ_PRM_EXT_TRIGGER_DELAY_TIME_BASE		CORACQ_VAL_TIME_BASE_LINE_VALID (0x4) CORACQ_VAL_TIME_BASE_LINE_TRIGGER (0x8) CORACQ_VAL_TIME_BASE_SHAFT_ENCODER (0x40) CORACQ_VAL_TIME_BASE_NS (0x80)
CORACQ_PRM_COLOR_DECODER_ENABLE	Base/Full Mono *10T8B/8T10B* *Base/Medium Color RGB* *Full Packed RGB* *Full Packed RGBY* *80B Packed RGB*	Not available
	Base/Full Bayer 10T8B Bayer 8T10B Bayer 80B Packed Bi-Color	TRUE FALSE
CORACQ_PRM_COLOR_DECODER_METHOD	Full Bayer 10T8B Bayer 8T10B Bayer	CORACQ_VAL_COLOR_DECODER_METHOD_1 (0x1)
	80B Packed Bi-Color	CORACQ_VAL_COLOR_DECODER_METHOD_7 (0x40)
CORACQ_PRM_WB_GAIN	Base/Full Color RGB Full Packed RGB 80B Packed RGB 80B Packed Bi-Color Base/Full Bayer 10T8B Bayer 8T10B Bayer	Min = 100000, max = 900000, step = 1
CORACQ_PRM_WB_GAIN_RED	Base/Full Color RGB Full Packed RGB 80B Packed RGB 80B Packed Bi-Color Base/Full Bayer 10T8B Bayer 8T10B Bayer	Min = 100000, max = 900000, step = 1
CORACQ_PRM_WB_GAIN_GREEN	Base/Full Color RGB Full Packed RGB 80B Packed RGB 80B Packed Bi-Color Base/Full Bayer 10T8B Bayer 8T10B Bayer	Min = 100000, max = 900000, step = 1

CORACQ_PRM_WB_GAIN_BLUE	Base/Full Color RGB Full Packed RGB 80B Packed RGB 80B Packed Bi-Color Base/Full Bayer 10T8B Bayer 8T10B Bayer	Min = 100000, max = 900000, step = 1
CORACQ_PRM_EXT_TRIGGER_IGNORE_DELAY		min = 0 µs max = 85899344 µs step = 1 µs
CORACQ_PRM_BOARD_SYNC_OUTPUT1_SOURCE (*)		min = 0 max = 10 step = 1
CORACQ_PRM_BOARD_SYNC_OUTPUT2_SOURCE (*)		min = 0 max = 10 step = 1
CORACQ_PRM_EXT_TRIGGER_SOURCE_STR		[0] = Automatic [1] = External Trigger #1 [2] = External Trigger #2 [3] = Board Sync #1 [4] = Board Sync #2 [5] = Software Trigger
CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE_STR		[0] = Automatic [1] = Shaft Encoder Phase A [2] = Shaft Encoder Phase B [3] = Shaft Encoder Phase A & B [4] = Board Sync #1 [5] = Board Sync #2
CORACQ_PRM_VERTICAL_TIMEOUT_DELAY		Not available
CORACQ_PRM_POCL_ENABLE		TRUE FALSE
CORACQ_PRM_SHAFT_ENCODER_DIRECTION		CORACQ_VAL_SHAFT_ENCODER_DIRECTION_IGNORE (0x00) CORACQ_VAL_SHAFT_ENCODER_DIRECTION_FORWARD (0x01) CORACQ_VAL_SHAFT_ENCODER_DIRECTION_REVERSE (0x02)
CORACQ_PRM_LINE_TRIGGER_AUTO_DELAY		CORACQ_VAL_LINE_TRIGGER_AUTO_DELAY_DISABLE (0x0) CORACQ_VAL_LINE_TRIGGER_AUTO_DELAY_FREQ_MAX (0x2)
CORACQ_PRM_TIME_STAMP_BASE		CORACQ_VAL_TIME_BASE_US (0x1) CORACQ_VAL_TIME_BASE_LINE_VALID (0X4) CORACQ_VAL_TIME_BASE_LINE_TRIGGER (0X8) CORACQ_VAL_TIME_BASE_SHAFT_ENCODER (0X40) CORACQ_VAL_TIME_BASE_100NS (0x200)
CORACQ_PRM_BOARD_SYNC_OUTPUT1_SOURCE_STR		[0] = Disabled [1] = External Frame Trigger [2] = Reserved [3] = CC1 [4] = CC2 [5] = CC3 [6] = CC4 [7] = Ext Trigger Ignore Region [8] = Shaft Encoder Before Mult/Drop [9] = Shaft Encoder After Mult/Drop [10] = Internal Line Trigger
CORACQ_PRM_BOARD_SYNC_OUTPUT2_SOURCE_STR		[0] = Disabled [1] = External Frame Trigger [2] = Reserved [3] = CC1 [4] = CC2 [5] = CC3 [6] = CC4 [7] = Ext Trigger Ignore Region [8] = Shaft Encoder Before Mult/Drop [9] = Shaft Encoder After Mult/Drop [10] = Internal Line Trigger
CORACQ_PRM_SHAFT_ENCODER_ORDER		CORACQ_VAL_SHAFT_ENCODER_ORDER_AUTO (0X0) CORACQ_VAL_SHAFT_ENCODER_ORDER_DROP_MULTIPLY (0X1) CORACQ_VAL_SHAFT_ENCODER_ORDER_MULTIPLY_DROP (0X2) * For auto mode, the order is multiply/drop.
CORACQ_PRM_CAM_FRAMES_PER_TRIGGER		Not available
CORACQ_PRM_LINE_INTEGRATE_TIME_BASE		CORACQ_VAL_TIME_BASE_PIXEL_CLK (0X100)
CORACQ_PRM_EXT_TRIGGER_IGNORE_REGION_DURATION		min = 0 µs max = 6553 µs step = 1 µs

CORACQ_PRM_STROBE_DESTINATION (*)	Not available

(*) Parameter Values are Board Specific

ACQ Related Parameters

Parameter		Values
CORACQ_PRM_LABEL	Base Mono Base Color RGB Base Bayer Full mono Medium Color RGB Full Packed RGB Full Bayer Full Packed RGBY 8T10B 10T8B 80B Packed RGB 80B Packed Bi-Color 10T8B Bayer 8T10B Bayer	Camera Link Base Mono Camera Link Base Color RGB Camera Link Base Bayer Camera Link Full Mono Camera Link Medium Color RGB Camera Link Full Packed RGB Camera Link Full Bayer Camera Link Full Packed RGBY Camera Link 8-Tap/10-Bit Mono Camera Link 10-Tap/8-Bit Mono Camera Link 80-Bit Packed RGB Camera Link 80-Bit Packed/8-Bit Bi-Color Camera Link 10-Tap/8-Bit Bayer Camera Link 8-Tap/10-Bit Bayer
CORACQ_PRM_EVENT_TYPE CORACQ_PRM_EVENT_TYPE_EX		CORACQ_VAL_EVENT_TYPE_START_OF_FRAME CORACQ_VAL_EVENT_TYPE_END_OF_FRAME CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER CORACQ_VAL_EVENT_TYPE_VERTICAL_SYNC CORACQ_VAL_EVENT_TYPE_NO_PIXEL_CLK CORACQ_VAL_EVENT_TYPE_PIXEL_CLK CORACQ_VAL_EVENT_TYPE_FRAME_LOST CORACQ_VAL_EVENT_TYPE_DATA_OVERFLOW CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_IGNORED CORACQ_VAL_EVENT_TYPE_EXT_LINE_TRIGGER_TOO_SLOW CORACQ_VAL_EVENT_TYPE_SHAFT_ENCODER_REVERSE_COUNT_OVERFLOW CORACQ_VAL_EVENT_TYPE_LINE_TRIGGER_TOO_FAST CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_END
CORACQ_PRM_SIGNAL_STATUS		CORACQ_VAL_SIGNAL_HSYNC_PRESENT CORACQ_VAL_SIGNAL_VSYNC_PRESENT CORACQ_VAL_SIGNAL_PIXEL_CLK_1_PRESENT CORACQ_VAL_SIGNAL_PIXEL_CLK_2_PRESENT CORACQ_VAL_SIGNAL_PIXEL_CLK_3_PRESENT CORACQ_VAL_SIGNAL_PIXEL_CLK_ALL_PRESENT CORACQ_VAL_SIGNAL_POWER_PRESENT CORACQ_VAL_SIGNAL_POCL_ACTIVE CORACQ_VAL_SIGNAL_POCL_ACTIVE_2
CORACQ_PRM_FLAT_FIELD_ENA BLE	Base Mono Full Mono 8T10B 10T8B	TRUE / FALSE
	Base Color RGB Base Bayer Medium Color RGB Full Packed RGB Full Packed RGBY Full Bayer 80B Packed RGB 80B Packed Bi-Color 10T8B Bayer 8T10B Bayer	Not Available
CORACQ_CAP_FLAT_FIELD_OFFSET	8-bit Mono	min = 0 max = 255 step = 1
	10-bit Mono	min = 0 max = 4095 step = 1
	12-bit Mono	min = 0 max = 16383 step = 1
	14-bit Mono	min = 0 max = 65535 step = 1
	16-bit Mono	Not Available

CORACQ_CAP_FLAT_FIELD_GAIN	8-bit Mono	min = 0 max = 255 step = 1
	10-bit Mono	min = 0 max = 4095 step = 1
	12-bit Mono	min = 0 max = 16383 step = 1
	14-bit Mono	min = 0 max = 65535 step = 1
	16-bit Mono	Not Available
CORACQ_CAP_FLAT_FIELD_GAIN_DIVISOR	8-bit Mono	128
	10-bit Mono	512
	12-bit Mono	2048
	14-bit Mono	8192
	16-bit Mono	Not Available
CORACQ_PRM_FLAT_FIELD_PIXEL_REPLACEMENT_METHOD		CORACQ_VAL_FLAT_FIELD_PIXEL_REPLACEMENT_METHOD_2 (Pixel replacement is done by averaging the 2 neighborhood pixels. When one of the neighbors is not available (border image pixels, the pixel is simply replaced with the available neighbor) CORACQ_VAL_FLAT_FIELD_PIXEL_REPLACEMENT_METHOD_3 (Pixel replacement is done by averaging neighborhood pixels using a 3x2 kernel)
CORACQ_PRM_FLAT_FIELD_SET_SELECT		min = 0 max = 16 step = 1
CORACQ_PRM_TIME_STAMP		Available
CORACQ_PRM_IMAGE_FILTER_ENABLE		Not Available
CORACQ_PRM_SHAFT_ENCODER_REVERSE_COUNT		Max = 65536 ticks
CORACQ_PRM_META_DATA		CORACQ_VAL_META_DATA_PER_LINE_RIGHT (0x2)
CORACQ_PRM_SHAFT_ENCODER_STATUS		CORACQ_VAL_SHAFT_ENCODER_STATUS_DIRECTION_FORWARD/CORACQ_VAL_SHAFT_ENCODER_STATUS_DIRECTION_REVERSE (0x1) CORACQ_VAL_SHAFT_ENCODER_STATUS_TOO_SLOW (0x2) CORACQ_VAL_SHAFT_ENCODER_STATUS_REVERSE_COUNT_OVERFLOW (0x4)
CORACQ_PRM_SHAFT_ENCODER_COUNT		Available
CORACQ_CAP_SERIAL_PORT_INDEX		Supported

Transfer Related Capabilities

Capability	Values
CORXFER_CAP_NB_INT_BUFFERS	CORXFER_VAL_NB_INT_BUFFERS_AUTO (0x2)
CORXFER_CAP_MAX_XFER_SIZE	4294967040 Bytes
CORXFER_CAP_MAX_FRAME_COUNT	16777215 Frames
CORXFER_CAP_COUNTER_STAMP_AVAILABLE	FALSE
CORXFER_CAP_TRANSFER_SYNC	CORXFER_VAL_TRANSFER_SYNC_SUPPORTED (0x1)

Transfer Related Parameters

Parameter	Values
CORXFER_PRM_EVENT_TYPE CORXFER_PRM_EVENT_TYPE_EX	CORXFER_VAL_EVENT_TYPE_START_OF_FRAME CORXFER_VAL_EVENT_TYPE_END_OF_FRAME CORXFER_VAL_EVENT_TYPE_END_OF_TRANSFER CORXFER_VAL_EVENT_TYPE_END_OF_LINE CORXFER_VAL_EVENT_TYPE_END_OF_NLINES
CORXFER_PRM_START_MODE	CORXFER_VAL_START_MODE_ASYNCHRONOUS (0x0) CORXFER_VAL_START_MODE_SYNCHRONOUS (0x1) CORXFER_VAL_START_MODE_HALF_ASYNCHRONOUS (0x2) CORXFER_VAL_START_MODE_SEQUENTIAL (0x3)
CORXFER_PRM_CYCLE_MODE	CORXFER_VAL_CYCLE_MODE_ASYNCHRONOUS (0x0) CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_WITH_TRASH (0x2) CORXFER_VAL_CYCLE_MODE_OFF (0x3) CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_NEXT_EMPTY_WITH_TRASH (0x5)
CORXFER_PRM_FLIP	CORXFER_VAL_FLIP_OFF (0x0) CORXFER_VAL_FLIP_VERT (0x2)
CORXFER_PRM_INT_BUFFERS	* Depends on acquired image size. By default driver will optimize the number of on-board buffers.
CORXFER_PRM_EVENT_COUNT_SOURCE	CORXFER_VAL_EVENT_COUNT_SOURCE_DST (0x1) CORXFER_VAL_EVENT_COUNT_SOURCE_SRC (0x2)
CORXFER_PRM_BUFFER_TIMESTAMP_MODULE	CORXFER_VAL_BUFFER_TIMESTAMP_MODULE_ACQ (0x1) CORXFER_VAL_BUFFER_TIMESTAMP_MODULE_XFER (0x13)
CORXFER_PRM_BUFFER_TIMESTAMP_EVENT (ACQ Related)	CORACQ_VAL_EVENT_TYPE_START_OF_FRAME (0x80000) CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER (0x1000000)
CORXFER_PRM_BUFFER_TIMESTAMP_EVENT (XFER Related)	CORXFER_VAL_EVENT_TYPE_END_OF_FRAME (0x800000)
CORXFER_PRM_LINE_MERGING	CORXFER_VAL_LINE_MERGING_AUTO (0x0) CORXFER_VAL_LINE_MERGING_OFF (0x2)

General Outputs #1: Related Capabilities (GIO Module #0)

These are the User Interface Outputs available on connector J1 and J4.

Capability	Values
CORGIO_CAP_IO_COUNT	Rev A1: 4 I/Os, Rev A2/A3/Bx: 8 I/Os
CORGIO_CAP_DIR_OUTPUT	0xf
CORGIO_CAP_DIR_TRISTATE	0xf
CORGIO_CAP_EVENT_TYPE	Not Available
CORGIO_CAP_READ_ONLY	0x03 (* depends on strobe outputs reserved for acquisition device)

General Outputs #1: Related Parameters (GIO Module #0)

Parameter	Values
CORGIO_PRM_LABEL	General Outputs #1
CORGIO_PRM_DEVICE_ID	0
CORGIO_PRM_OUTPUT_TYPE	CORGIO_VAL_OUTPUT_TYPE_LVTTL (0x20)
CORGIO_PRM_CONNECTOR	CORGIO_VAL_CONNECTOR_1 (0x1)

General Inputs #1: Related Capabilities (GIO Module #1)

These are the User Interface Inputs available on connector J1 and J4.

Capability	Values
CORGIO_CAP_IO_COUNT	4 I/Os
CORGIO_CAP_DIR_OUTPUT	0x0
CORGIO_CAP_DIR_TRISTATE	0x0
CORGIO_CAP_EVENT_TYPE	CORGIO_VAL_EVENT_TYPE_RISING_EDGE (0x1) CORGIO_VAL_EVENT_TYPE_FALLING_EDGE (0x2)
CORGIO_CAP_READ_ONLY	0x03 (* depends on external trigger inputs reserved for acquisition device)

General Inputs #1: Related Parameters (GIO Module #1)

Parameter	Values
CORGIO_PRM_LABEL	General Inputs #1
CORGIO_PRM_DEVICE_ID	1
CORGIO_PRM_INPUT_LEVEL	CORGIO_VAL_INPUT_LEVEL_TTL (0x1) CORGIO_VAL_INPUT_LEVEL_422 (0x2) CORGIO_VAL_INPUT_LEVEL_24VOLTS (0x8) CORGIO_VAL_INPUT_LEVEL_12VOLTS (0x40)
CORGIO_PRM_CONNECTOR	CORGIO_VAL_CONNECTOR_1 (0x1)

Bidirectional General I/Os: Related Capabilities (GIO Module #2)

These are the Open Interface I/Os available on connector J5.

Capability	Values
CORGIO_CAP_IO_COUNT	8 I/Os
CORGIO_CAP_DIR_OUTPUT	0xff
CORGIO_CAP_DIR_TRISTATE	0xff
CORGIO_CAP_EVENT_TYPE	Not Available
CORGIO_CAP_READ_ONLY	0x03 (* depends on board syncs reserved for acquisition device)

Bidirectional General I/Os: Related Parameters (GIO Module #2)

Parameter	Values
CORGIO_PRM_LABEL	Bidirectional General I/Os #1
CORGIO_PRM_DEVICE_ID	2
CORGIO_PRM_OUTPUT_TYPE	CORGIO_VAL_OUTPUT_TYPE_LVTTL (0x20)
CORGIO_PRM_INPUT_LEVEL	CORGIO_VAL_INPUT_LEVEL_LVTTL (0x20)
CORGIO_PRM_CONNECTOR	CORGIO_VAL_CONNECTOR_2 (0x2)

Sapera Servers & Resources

Servers and Resources

The following table describes services and resources available for the Xtium-CL MX4 board.

Servers	Resources			
Name	**Type**	**Name**	**Index**	**Description**
Xtium-CL_MX4_1 (Full firmware)	Acquisition	Camera Link Full Mono	0	Base, Medium and Full configuration, Monochrome Camera
		Camera Link Medium Color RGB	1	Base and Medium configuration, RGB Camera
		Camera Link Full Packed RGB	2	Full packed 8-bit RGB Camera
		Camera Link Full Bayer	3	Base, Medium and Full configuration, Bayer Camera
		Camera Link Full Packed RGBY	4	Full packed 8-bit RGBY Camera
Xtium-CL_MX4_1 (Dual firmware)	Acquisition	Camera Link Base Mono #1	0	Base Monochrome Camera #1
		Camera Link Base Mono #2	1	Base Monochrome Camera #2
		Camera Link Base Color RGB #1	2	Base RGB Camera #1
		Camera Link Base Color RGB #2	3	Base RGB Camera #2
		Camera Link Base Bayer #1	4	Base Bayer Camera #1
		Camera Link Base Bayer #2	5	Base Bayer Camera #2
Xtium-CL_MX4_1 (80-bit firmware)	Acquisition	Camera Link 10-Tap/8-Bit Mono	0	80-bit configuration, Monochrome 10 Taps @ 8 bits Camera
		Camera Link 8-Tap/10-Bit Mono	1	80-bit configuration, Monochrome 8 Taps @ 10 bits Camera
		Camera Link 80-Bit Packed RGB	2	80-bit configuration, RGB 80-bit packed 8/12-bit Camera
		Camera Link 80-Bit Packed/8-Bit Bi-Color	3	80-bit configuration, Bi-Color 80-bit packed 8-bit Camera
		Camera Link 10-Tap/8-Bit Bayer	4	80-bit configuration, Bayer 10 Taps @ 8 bits Camera
		Camera Link 8-Tap/10-Bit Bayer	5	80-bit configuration, Bayer 8 Taps @ 10 bits Camera
All	GIO	General Outputs #1	0	8 General Outputs (4 on Rev A1)
		General Inputs #1	1	4 General Inputs
		Bidirectional General I/Os #1	2	8 Bidirectional General I/Os

Windows Embedded 7 Installation

Windows Embedded 7 is not officially supported by Teledyne DALSA due to the number of possible configurations. However, Sapera LT and other Teledyne DALSA products should function properly on the Windows Embedded 7 platform provided that the required components are installed.

Teledyne DALSA provides answer files (.xml) for use during Windows Embedded 7 installation that install all necessary components for running Sapera LT 32-bit or 64-bit versions (SDK or Runtime), Sapera Processing 32-bit or 64-bit versions (SDK or Runtime), and Teledyne DALSA frame grabbers.

For each platform (32 or 64-bit), the answer file provided is:

- **SaperaFrameGrabbers.xml**:
  Configuration for Sapera LT, Sapera Processing and Teledyne DALSA framegrabbers

The file is located in the following directory dependent on the platform used:

```
<Install Directory>\Sapera\Install\Win7_Embedded\Win32
<Install Directory>\Sapera\Install\Win7_Embedded\Win64
```

The OS footprint for these configurations is less than 1 GB. Alternatively, the Windows Thin Client configuration template provided by Microsoft in the Windows Embedded 7 installation also provides the necessary dependencies for Sapera LT, and Teledyne DALSA framegrabbers (with an OS footprint of approximately 1.5 GB).

If you are installing other applications on the Windows Embedded 7 platform, it is recommended that you verify which components are required, and if necessary, create a corresponding “Answer File”.

For more information on performing dependency analysis to enable your application on Windows Embedded 7, refer to the Microsoft Windows Embedded 7 documentation.

Technical Specifications

Xtium-CL MX4 Board Specifications

Digital Video Input & Controls

Input Type	Camera Link Specifications Rev 2.0 compliant; 2 Base or 1 Full or 1 Medium or 1 80-bit (using SDR-26 Camera Link connectors — MiniCL) Supports PoCL cameras in: Camera Link Base, Medium, Full/80-Bit Configurations
Common Pixel Formats	Camera Link tap configuration: 8, 10, 12, 14 and 16-bit mono 8, 10, 12-bit RGB 8, 10, 12-bit Bayer 8-bit Bi-Color
Tap Format Details	1 Tap – 8/10/12/14/16-bit mono 2 Taps – 8/10/12-bit mono 3 Taps – 8/10/12-bit mono 4 Taps – 8/10/12-bit mono 8 Taps – 8-bit mono 8 Taps – 10-bit mono 10 Taps – 8-bit mono 1 Tap – 8/10/12-bit RGB 2 Taps – 8-bit RGB Full packed 8-bit RGB/BGR Full packed 8-bit RGBY 80-bit packed 8/12-bit RGB/BGR 80-bit packed 8-bit Bi-Color
Scanning	Area scan and Line scan: Progressive, Segmented, Multi-Tap, Tap reversal, Alternate Tap Configuration, Dual Channel
Scanning Directions	Left to Right, Right to Left, Up-Down, From Top
Resolution *note: these are Xtium-CL MX4 maximums, not Camera Link specifications*	Horizontal Minimum: 8 Pixels per tap (8-bits/pixel) Horizontal Maximum: 8-bits/pixel x 64k Pixels/line 16-bits/pixel x 32k Pixels/line 32-bits/pixel x 16k Pixels/line 64-bits/pixel x 8k Pixels/line Vertical Minimum: 1 line Vertical Maximum: up to 65536 lines—for area scan sensors infinite line count—for line scan sensors
Pixel Clock Range	20 MHz to 85 MHz
Synchronization Minimums	Horizontal Sync minimum: 1 pixel Vertical Sync minimum: 1 line
Image Buffer	Available with 512 MB
Bandwidth to Host System	Approximately 1.7GB/s (maximum obtained is dependent on firmware loaded and PC characteristics)
Serial Port	Supports communication speeds from 9600 to 921600 bps

Controls	Compliant with Teledyne DALSA Trigger-to-Image Reliability framework Comprehensive event notifications Timing control logic for camera triggers and strobe signals External trigger latency less than 100 nsec Supports multi-board / multi-camera synchronization Quadrature (phase A & B) shaft encoder inputs for external web synchronization: RS-422 or TTL (Rev B Only) input (mutually exclusive) maximum frequency is 5 MHz 4 differential opto-coupled general inputs (RS-422/TTL/12V/24V). Can be used as opto-coupled external trigger inputs programmable as active high or low (edge or level trigger). (only 1 input can be connected to a differential input signal on Rev A1) 8 LVTTL general outputs. Can be used as Strobe outputs. (4 on Rev A1) I/O available on a DH60-27P connector (J1) and on 26-pin SHF-113-01-L-D-RA (J4)
POCL	Overcurrent circuit protection: PTC (Positive Temperature Coefficient): 2 on the board, one each for the 2 PoCL circuits. PTCs are limited to 0.5A (hold) and 1A (trip) @ 25C. Part used is Littelfuse’s 1210L050.
Processing *Dependant on user loaded firmware configuration*	Output Lookup Table Bayer Mosaic Filter Bi-Color Conversion (for TDALSA P4) Flat Field/Flat Line Correction
Certifications	EC & FCC (see EMI Certifications) RoHs (Restriction of Hazardous Substances) REACH (Registration, Evalulation Authorization and Restriction of Chemicals) China RoHS UL94 (Standard for Safety of Flammability) (PCB only)

Host System Requirements

Xtium-CL MX4 Dimensions

Approximately 4 in. (10 cm) wide by 4 in. (10 cm) high

General System Requirements for the Xtium-CL MX4

- PCI Express Gen2 x4 slot compatible;
  (will work in Gen1 x4 slot with reduced bandwidth to host)
- On some computers the Xtium-CL MX4 may function installed in a x16 slot. The computer documentation or direct testing by the user is required.
- Xtium-CL MX4 operates correctly when installed in a multi-processor system (including Hyper-Threading multi-core processors).

Operating System Support

Windows 7, Windows 8 and Windows 10, each in either 32-bit or 64-bit

Environment

Ambient Temperature:	10° to 50°C (operation) -40° to 75°C (storage)
Relative Humidity:	5% to 90% non-condensing (operating) 0% to 95% (storage)
MTBF @40°C	36.4 years

Note: Ensure adequate airflow for proper functioning of the board across the entire temperature range of 10 – 50°C . Airflow measuring 80 LFM (linear feet per minute) across the surface of the board is recommended.

Power Requirements during Acquisitions

PC Voltage	Rev A1	Rev A2/A3/Bx
+3.3V	0.9A	N/A (Regulator used to generate the 3.3V from 12V)
+12V	0.54A	0.80

EMI Certifications

TELEDYNE DALSA
Everywhereyoulook™

EC & FCC DECLARATION OF CONFORMITY

We :
Teledyne DALSA inc.
880 Rue McCaffrey
St-Laurent, Québec
Canada H4T 2C7

Declare under sole legal responsibility that the following products conform to the protection requirements of council directive 2004/108/EC (2014/30/EU after April 2016) on the approximation of the laws of member states relating to electromagnetic compatibility:

Xtium-CL MX4

The products to which this declaration relates are in conformity with the following relevant harmonized standards, the reference numbers of which have been published in the Official Journal of the European Communities:

EN55032 (2012)	Electromagnetic compatibility of multimedia equipment — Emission requirements
EN55011 (2009) with A1(2010)	Industrial, scientific and medical equipment — Radio-frequency disturbance characteristics — Limits and methods of measurement
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use — EMC requirements — Part 1: General requirements
EN 55024 (2010)	Information technology equipment — Immunity characteristics — Limits and methods of measurement

Further declare under our sole legal responsibility that the product listed also conforms to the following international standards:

CFR 47	part 15 (2008), subpart B, for a class A product. Limits for digital devices
ICES-003	Information Technology Equipment (ITE) — Limits and Methods of Measurement
CISPR 11	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement
CISPR 32	Electromagnetic compatibility of multimedia equipment - Emission requirements

Note: this product is intended to be a component of a larger system.

St-Laurent, Canada — 2015-03-18
Location — Date

Hank Helmond.
Director, Quality Assurance

Figure 23: EMI Certifications

Connector and Switch Locations

Xtium-CL MX4 Board Layout Drawing

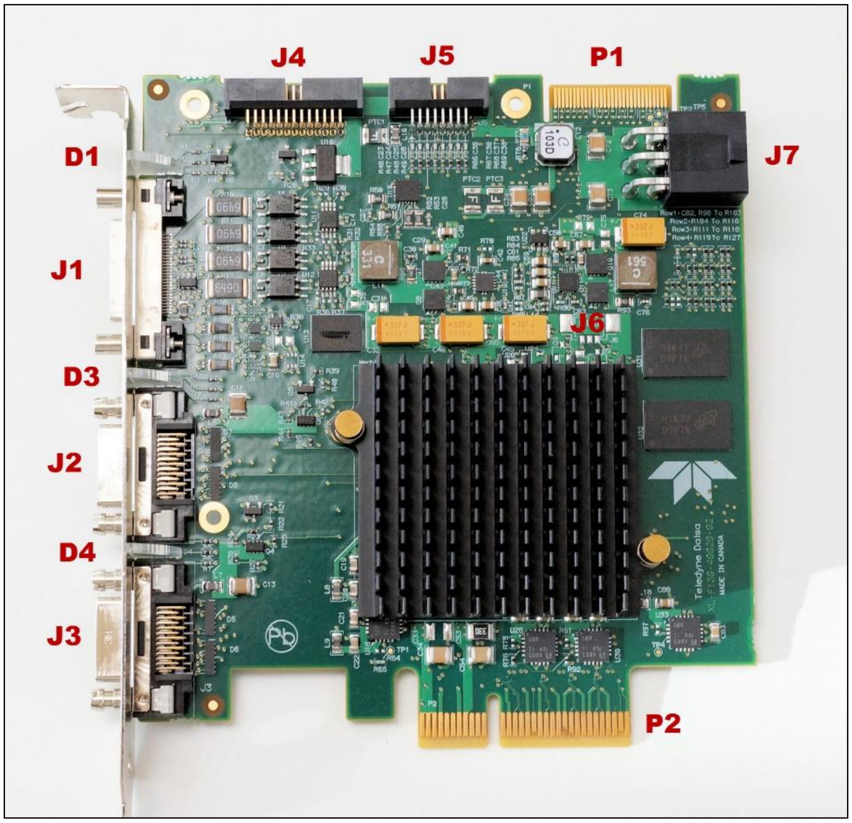


Figure 24: Board Layout

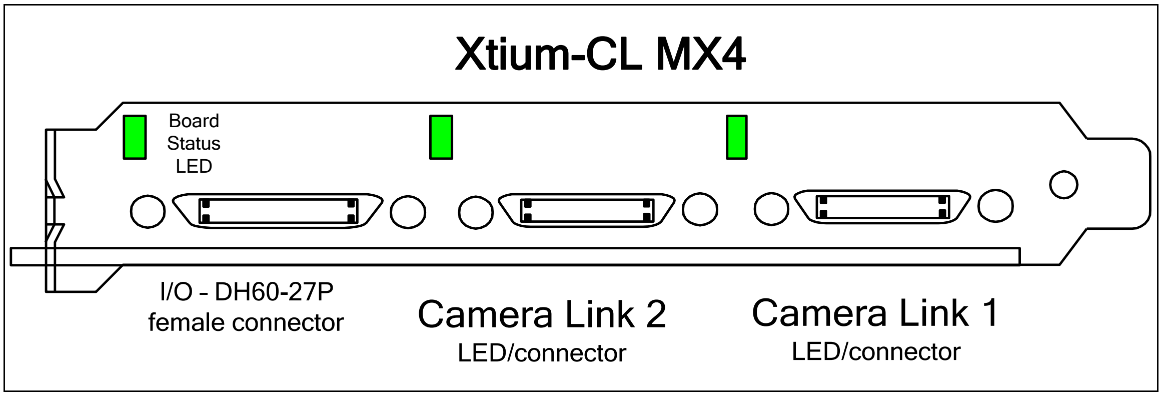
Connector / LED Description List

The following table lists components on the Xtium-CL MX4 board. Detailed information concerning the connectors/LEDs follows this summary table.

Location	Description	Location	Description
J1	External Signals connector DH60-27P	J5	Multi Board Sync
J2	Camera Link 2 Connector	J7	PC power to camera interface and/or J1
J3	Camera Link 1 Connector	D1	Boot-up/PCIe Status LED (refer to text)
P2	PCIe x4 computer bus connector (Gen2 compliant slot preferred)	D3, D4	Camera status LEDs
J4	Internal I/O Signals connector (26-pin SHF-113-01-L-D-RA)	J6, P1	Reserved

Connector and Switch Specifications

Xtium-CL MX4 End Bracket Detail



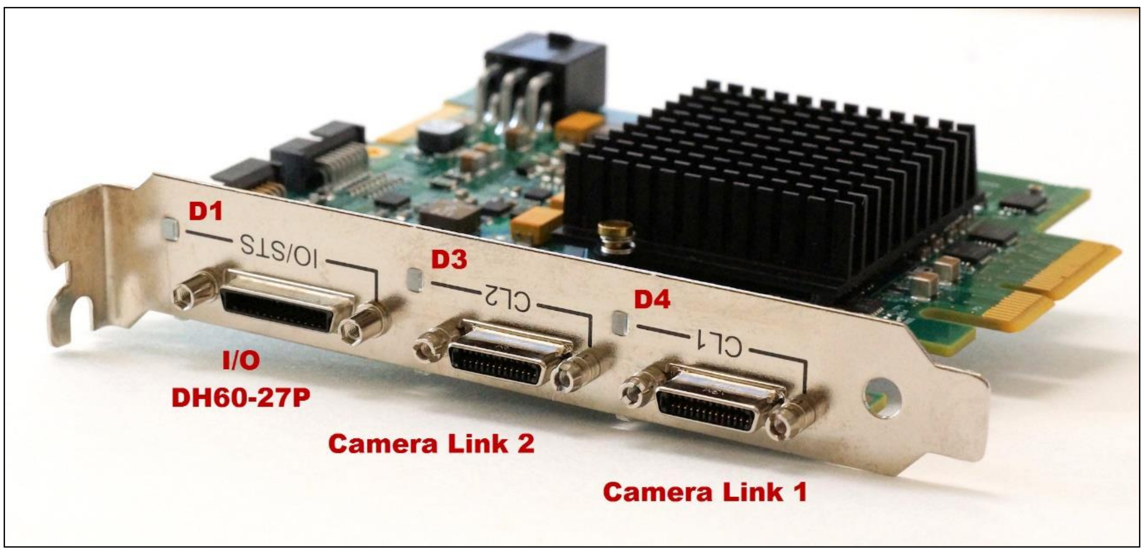


Figure 25: End Bracket Details

The hardware installation process is completed with the connection of a supported camera to the Xtium-CL MX4 board using Camera Link cables (see Camera Link Cable).

- The Xtium-CL MX4 board supports a camera with one or two Camera Link connectors (one Base, one Medium or one Full – see Data Port Summary for information on Camera Link configurations).
- Connect the camera to the J3 connector with a Camera Link cable. When using a Medium or Full camera, connect the second camera connector to J2.

	Note: If the camera is powered by the Xtium-CL MX4, refer to J7: Power Connector for power connections.

Contact Teledyne DALSA or browse our web site www.teledynedalsa.com/mv for information on Xtium-CL MX4 supported cameras.

Status LED Functional Description

D1 Boot-up/PCIe status LED

Color	State	Description
Red	Solid	FPGA firmware not loaded
Green	Solid	Normal FPGA firmware loaded, Gen2 speed, link width x4
Green	Flashing	Normal FPGA firmware loaded, Gen1 speed, link width x4
Yellow	Solid	Normal FPGA firmware loaded, Gen2 speed, link width not x4
Yellow	Flashing	Normal FPGA firmware loaded, Gen1 speed, link width not x4
Blue	Solid	Safe FPGA firmware loaded, Gen2 speed
Blue	Flashing	Safe FPGA firmware loaded, Gen1 speed
Red	Flashing	PCIe Training Issue – Board will not be detected by computer

Camera Link LEDs
(D4 = Camera Link connector #1, D3 = Camera Link connector #2)

Color	State	Description
Red	Solid	No Camera Link pixel clock detected
Green	Solid	Camera Link pixel clock detected. No line valid detected. Note: for D3, when configuring for Full Camera Link, both pixel clock on the 2nd cable must be detected.
Green	Slow Flashing ~1 Hz	Camera Link pixel clock and line valid signal detected Note: for D3, when configuring for Full Camera Link, both line valid on the 2nd cable must be detected.
Green	Fast Flashing ~8 Hz	Acquisition in progress

- Notes 1: When using a Full configuration, if the input on CL1 is configured as Camera Link Base, the D3 (for CL2) will remain RED at all times.
- Note 2: LED D3 and D4 are independent.
- Note 3: Full FPGA defaults to Camera Link Medium configuration.
- Note 4: For a Pixel Clock and Line Valid to be detected, the following rules apply:
    - CL1: Requires 1 clock and 1 LVAL
    - CL2: Camera Link Base configuration: N/A
    - CL2: Camera Link Medium configuration requires 1 clock and 1 LVAL
    - CL2: Camera Link Full/80-bit configurations requires 2 clocks and 2 LVAL

J3: Camera Link Connector 1

Name	Pin #	Type	Description
BASE_X0-	25	Input	Neg. Base Data 0
BASE_X0+	12	Input	Pos. Base Data 0
BASE_X1-	24	Input	Neg. Base Data 1
BASE_X1+	11	Input	Pos. Base Data 1
BASE_X2-	23	Input	Neg. Base Data 2
BASE_X2+	10	Input	Pos. Base Data 2
BASE_X3-	21	Input	Neg. Base Data 3
BASE_X3+	8	Input	Pos. Base Data 3
BASE_XCLK-	22	Input	Neg. Base Clock
BASE_XCLK+	9	Input	Pos. Base Clock
SERTC+	20	Output	Pos. Serial Data to Camera
SERTC-	7	Output	Neg. Serial Data to Camera
SERTFG-	19	Input	Neg. Serial Data to Frame Grabber
SERTFG+	6	Input	Pos. Serial Data to Frame Grabber
CC1-	18	Output	Neg. Camera Control 1
CC1+	5	Output	Pos. Camera Control 1
CC2+	17	Output	Pos. Camera Control 2
CC2-	4	Output	Neg. Camera Control 2
CC3-	16	Output	Neg. Camera Control 3
CC3+	3	Output	Pos. Camera Control 3
CC4+	15	Output	Pos. Camera Control 4
CC4-	2	Output	Neg. Camera Control 4
PoCL	1,26		+12 V (see note following table)
GND	13, 14		Ground

Notes on PoCL support:

- Refer to Sapera's parameter CORACQ_PRM_POCL_ENABLE to enable PoCL and CORACQ_PRM_SIGNAL_STATUS/CORACQ_VAL_SIGNAL_POCL_ACTIVE to verify if the POCL is active. See also Sapera++ reference parameter SapAcquisition::SignalPoCLActive for the current state.
- PoCL state is maintained as long as the board is not reset

J2: Camera Link Connector 2

Medium and Full Camera Link sources require cables connected to both J2 and J3.

Name	Pin #	Type	Description
MEDIUM _X0-	25	Input	Neg. Medium Data 0
MEDIUM _X0+	12	Input	Pos. Medium Data 0
MEDIUM _X1-	24	Input	Neg. Medium Data 1
MEDIUM _X1+	11	Input	Pos. Medium Data 1
MEDIUM _X2-	23	Input	Neg. Medium Data 2
MEDIUM _X2+	10	Input	Pos. Medium Data 2
MEDIUM _X3-	21	Input	Neg. Medium Data 3
MEDIUM _X3+	8	Input	Pos. Medium Data 3
MEDIUM _XCLK-	22	Input	Neg. Medium Clock
MEDIUM _XCLK+	9	Input	Pos. Medium Clock
TERM	20		Term Resistor
TERM	7		Term Resistor
FULL_X0-	19	Input	Neg. Full Data 0
FULL _X0+	6	Input	Pos. Full Data 0
FULL _X1-	18	Input	Neg. Full Data 1
FULL _X1+	5	Input	Pos. Full Data 1
FULL _X2-	17	Input	Neg. Full Data 2
FULL _X2+	4	Input	Pos. Full Data 2
FULL _X3-	15	Input	Neg. Full Data 3
FULL _X3+	2	Input	Pos. Full Data 3
FULL _XCLK-	16	Input	Neg. Full Clock
FULL _XCLK+	3	Input	Pos. Full Clock
PoCL	1,26		+12 V (see note following table)
GND	13, 14		Ground

Notes on PoCL support:

- Refer to Sapera's parameter CORACQ_PRM_POCL_ENABLE to enable PoCL and CORACQ_PRM_SIGNAL_STATUS/CORACQ_VAL_SIGNAL_POCL_ACTIVE_2 to verify if the POCL is active. See also Sapera++ reference parameter SapAcquisition::SignalPoCLActive for the current state.
- PoCL state is maintained as long as the board is not reset

Camera Link Camera Control Signal Overview

Four LVDS pairs are for general-purpose camera control, defined as camera inputs / frame grabber outputs by the Camera Link Base camera specification. These controls are on J3 connector.

- Camera Control 1 (CC1)
- Camera Control 2 (CC2)
- Camera Control 3 (CC3)
- Camera Control 4 (CC4)

Each camera manufacture is free to define the signals input on any one or all 4 control signals. These control signals are used either as camera control pulses or as a static logic state. Control signals not required by the camera are simply assigned as not used. Refer to your camera's user manual for information on what control signals are required.

Note 1: The Xtium-CL MX4 pulse controller has a minimum resolution of 20ns.
Note 2: The internal line trigger frequency has a 2μs resolution.

The Xtium-CL MX4 can assign any camera control signal to the appropriate Camera Link control. The following screen shot shows the Sapera CamExpert dialog where Camera Link controls are assigned (signals shown are not specific to any camera).

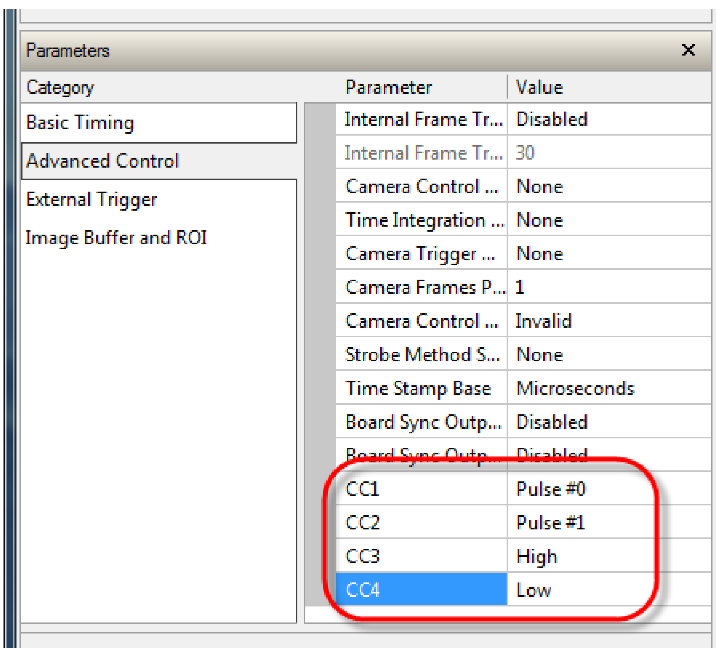


Figure 26: CamExpert - Camera Link Controls

J1: External Signals Connector (Female DH60-27P)

Warning: J1 and J4 have the same pinout assignment. Signals are routed to both connectors directly from their internal circuitry. Therefore never connect both J1 and J4 to external devices at the same time.

See DH40-27S Cable to Blunt End (OR-YXCC-27BE2M1, Rev B1) and Cable assemblies for I/O connector J4 for available cables.

J4: Internal I/O Signals Connector (26-pin SHF-113-01-L-D-RA)

Important: The table below describes the I/O signals available on both J1 and J4. (*applies to* ***Xtium-CL MX4 rev. B0***)

Use only one of the two I/O connectors — never both!

Xtium-CL MX4 rev. B0

Description	Pin #	Pin #	Description
Ground	1	15	General Input 3 (+)
RS-422 Shaft Encoder Phase A (-)	2	16	General Input 4 (+)
TTL/RS-422 Shaft Encoder Phase A (+) (*see note 3*)	3	17	General Input 4 (-)
Ground	4	18	General Input 3 (-)
RS-422 Shaft Encoder Phase B (-)	5	19	Power Output 5 Volts, 100mA max
TTL/RS-422 Shaft Encoder Phase B (+)	6	20	External Trigger Input 2 or General Input 2 (-)
External Trigger Input 1/General Input 1 (-)	7	21	General Output 3
External Trigger Input 1/General Input 1 (+)	8	22	General Output 4
External Trigger Input 2/General Input 2 (+)	9	23	General Output 5
Ground	10	24	General Output 6
Strobe 1 / General Output 1 (*See note 2*)	11	25	General Output 7
Strobe 2 / General Output 2 (*See note 2*)	12	26	General Output 8
Ground	13	27	NC
Power Output 12 Volts, 350mA max (*from Aux Power Connector, see J7)*	14		

Important: The table below describes the I/O signals available on both J1 and J4. (*applies to* ***Xtium-CL MX4 rev. A2/A3***)

Use only one of the two I/O connectors — never both!

Xtium-CL MX4 rev. A2/A3

Description	Pin #	Pin #	Description
Ground	1	15	General Input 3 (+)
RS-422 Shaft Encoder Phase A (-)	2	16	General Input 4 (+)
RS-422 Shaft Encoder Phase A (+) (*see note 3*)	3	17	General Input 4 (-)
Ground	4	18	General Input 3 (-)
RS-422 Shaft Encoder Phase B (-)	5	19	Power Output 5 Volts, 100mA max
RS-422 Shaft Encoder Phase B (+)	6	20	External Trigger Input 2 or General Input 2 (-)
External Trigger Input 1/General Input 1 (-)	7	21	General Output 3
External Trigger Input 1/General Input 1 (+)	8	22	General Output 4
External Trigger Input 2/General Input 2 (+)	9	23	General Output 5
Ground	10	24	General Output 6
Strobe 1 / General Output 1 (*See note 2*)	11	25	General Output 7
Strobe 2 / General Output 2 (*See note 2*)	12	26	General Output 8
Ground	13	27	NC
Power Output 12 Volts, 350mA max (*from Aux Power Connector, see J7)*	14		

Important: The table below describes the I/O signals available on both J1 and J4. (*applies to* ***Xtium-CL MX4 rev. A1***)

Use only one of the two I/O connectors — never both!

Xtium-CL MX4 rev. A1

Description	Pin #	Pin #	Description
Ground	1	15	General Input 3
RS-422 Shaft Encoder Phase A (-)	2	16	General Input 4
RS-422 Shaft Encoder Phase A (+) (*see note 3*)	3	17	Reserved
Ground	4	18	Reserved
RS-422 Shaft Encoder Phase B (-)	5	19	Reserved
RS-422 Shaft Encoder Phase B (+)	6	20	Reserved
General Input Common External Trigger Input 1 (-) General Input 1 (-)	7	21	General Output 3
External Trigger Input 1 (+) General Input 1 (+) (*Opto-coupled — see note 1*)	8	22	General Output 4
External Trigger Input 2 General Input 2	9	23	Reserved
Ground	10	24	Reserved
Strobe 1 General Output 1 (*See note 2*)	11	25	Reserved
Strobe 2 General Output 2	12	26	Reserved
Ground	13	27	Reserved
Power Output 12 Volts, 350mA max (*from Aux Power Connector, see J7 below*)	14		

Note 1: General Inputs / External Trigger Inputs Specifications

Each of the four General Inputs are opto-coupled and able to connect to differential or single ended source signals. General Input 1 and 2 can also act as External Trigger Inputs. See "Board Information" user settings. These inputs generate individual interrupts and are read by the Sapera application.

- Note: On Rev A1, only General Input 1 can be connected to a differential source signal.

The following figure is typical for each Genera Input. General Input 1 can be connected to a differential input signal. **Note** that in this specific case, the other 3 General Inputs cannot be used.

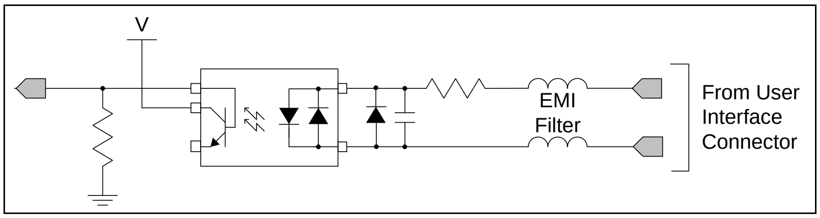


Figure 27: General Inputs Electrical Diagram

Input Details:

- Maximum input voltage is 26V.
- Maximum input signal frequency is 100 KHz.
- Each input has a 649-ohm series resistor on the opto-coupler input.
- The 0.01uF capacitor provides high frequency noise filtering.
- Minimum current is dependent on input voltage applied: $I_{optoin}(min) = (V_{optoin} - 0.5)/649\Omega$
- The switch point is software programmable to support differential (LVDS/RS422) or single ended TTL, 12V or 24V input signals.

For External Trigger usage:

- Input signal is "debounced" to ensure that no voltage glitch is detected as a valid transition. This debounce circuit time constant can be programmed from 1µs to 255µs. Any pulse smaller than the programmed value is blocked and therefore not seen by the board. If no debounce value is specified (value of 0µs), the minimum value of 1µs will be used.
- Refer to Sapera parameters:
  CORACQ_PRM_EXT_TRIGGER_SOURCE
  CORACQ_PRM_EXT_TRIGGER_ENABLE
  CORACQ_PRM_EXT_TRIGGER_LEVEL
  CORACQ_PRM_EXT_FRAME_TRIGGER_LEVEL
  CORACQ_PRM_EXT_TRIGGER_DETECTION
  CORACQ_PRM_EXT_TRIGGER_DURATION
- See also *.cvi file entries:
  External Trigger Level, External Frame Trigger Level, External Trigger Enable, External Trigger Detection.
- External Trigger Input 2 used for two pulse external trigger with variable frame length line scan acquisition.

Trigger Signal Total Delay

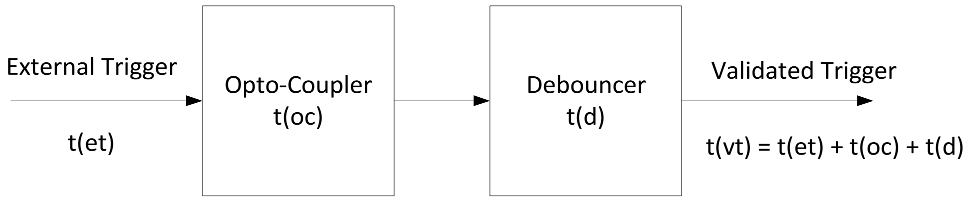


Figure 28: External Trigger Input Validation & Delay

External Trigger Timing Specifications	
t(et)	time of external trigger in µs
t(oc)	time opto-coupler takes to change state (time varies dependent on input voltage)
t(d)	user set debounce duration from 1 to 255µs
t(vt)	time of validated trigger in µs

Note: Teledyne DALSA recommends using the fastest transition to minimize the time it takes for the opto-coupler to change state.

If the duration of the external trigger is > t(oc) + t(d), then a valid acquisition trigger is detected.

It is possible to emulate an external trigger using the software trigger which is generated by a function call from an application.

The following table provides the input switching points and propagation delay details.

Trigger Level	Switch Point	Propagation Delay t(oc) (*rising edge signal* ↑)	Propagation Delay t(oc) (*falling edge signal* ↓)
RS-422	1.6V	1.75 µs	5.5 µs
TTL	1.6V	1.75 µs	5.5 µs
12V	6V	2.6 µs	2.6 µs
24V	12V	1.9 µs	3.1 µs

Block Diagram: Connecting External Drivers to General Inputs on J1 or J4

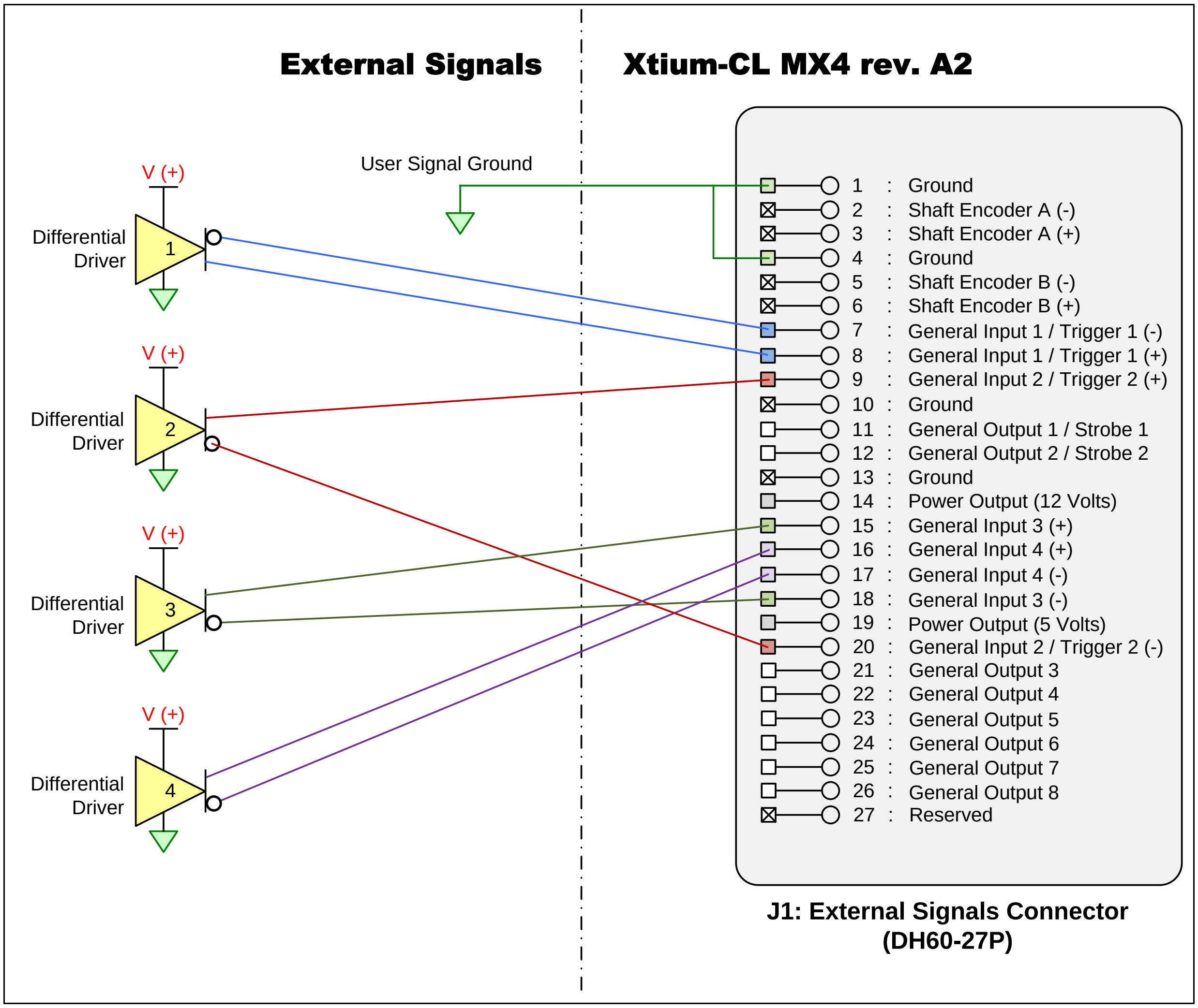


Figure 29:Rev A2/A3/Bx: External Signals Connection Diagram

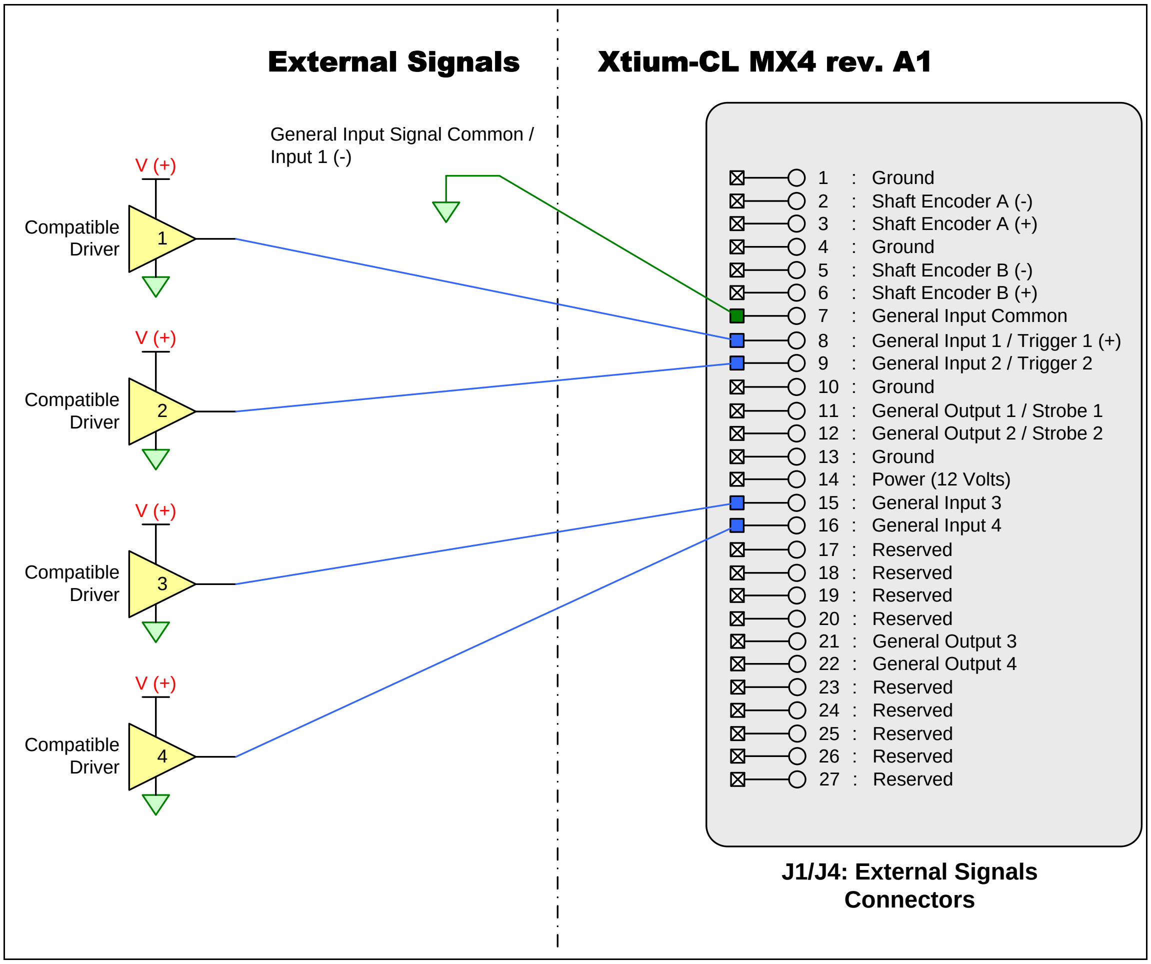


Figure 30:Rev A1: External Signals Connection Diagram

External Driver Electrical Requirements

The Xtium-CL allows user selected (software programmable) input switching points to support differential (RS-422) input signals and single ended (TTL, 12V, 24V) input signals. The following table defines the external signal voltage requirements from the driver circuits connected to the Xtium external inputs.

Input Level	Description	MIN	MAX
RS-422	Output Voltage High (V_{OH})	2.4 V	13.0 V
	Output Voltage Low (V_{OL})	-2.4 V	-13.0 V
TTL	Output Voltage High (V_{OH})	2.4 V	5.5 V
	Output Voltage Low (V_{OL})	0 V	0.8 V
12V	Output Voltage High (V_{OH})	9 V	13.2 V
	Output Voltage Low (V_{OL})	0 V	3 V
24V	Output Voltage High (V_{OH})	18 V	26.4 V
	Output Voltage Low (V_{OL})	0 V	6 V

Note 2: General Outputs /Strobe Output Specifications

Each of the eight General Outputs are TTL (3.3V) compatible. General Output 1 and 2 also function as the Strobe Output 1 and 2 respectively controlled by Sapera strobe control functions. See "Board Information" user settings. The following figure is typical for each General Output.

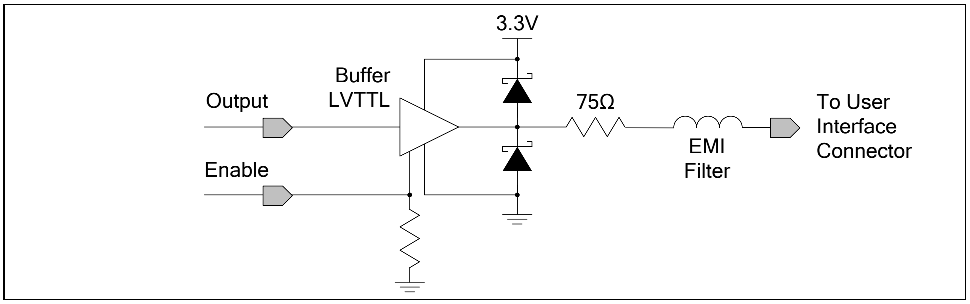


Figure 31: General Outputs Electrical Diagram

Output Details:

- Each output has a 75-ohm series resistor
- The 2 diodes protects the LVTTL buffer against overvoltage
- Each output is a tri-state driver, enabled by software
- Minimum guaranteed output current is +/- 24mA @ 3.3V
- Maximum output current is 50mA
- Maximum short circuit output current is 44mA
- Minimum voltage for output level high is 2.4V, while maximum voltage for output low is 0.55V
- Maximum output switching frequency is limited by driver and register access on the PCIe bus.

For Strobe Usage:

- Refer to Sapera Strobe Methods parameters:
  CORACQ_PRM_STROBE_ENABLE
  CORACQ_PRM_STROBE_POLARITY
  CORACQ_PRM_STROBE_LEVEL
  CORACQ_PRM_STROBE_METHOD
  CORACQ_PRM_STROBE_DELAY
  CORACQ_PRM_STROBE_DURATION
- See also *.cvi file entries:
  Strobe Enable, Strobe Polarity, Strobe Level, Strobe Method, Strobe Delay, Strobe Duration.

Block Diagram: Connecting External Receivers to the General Outputs

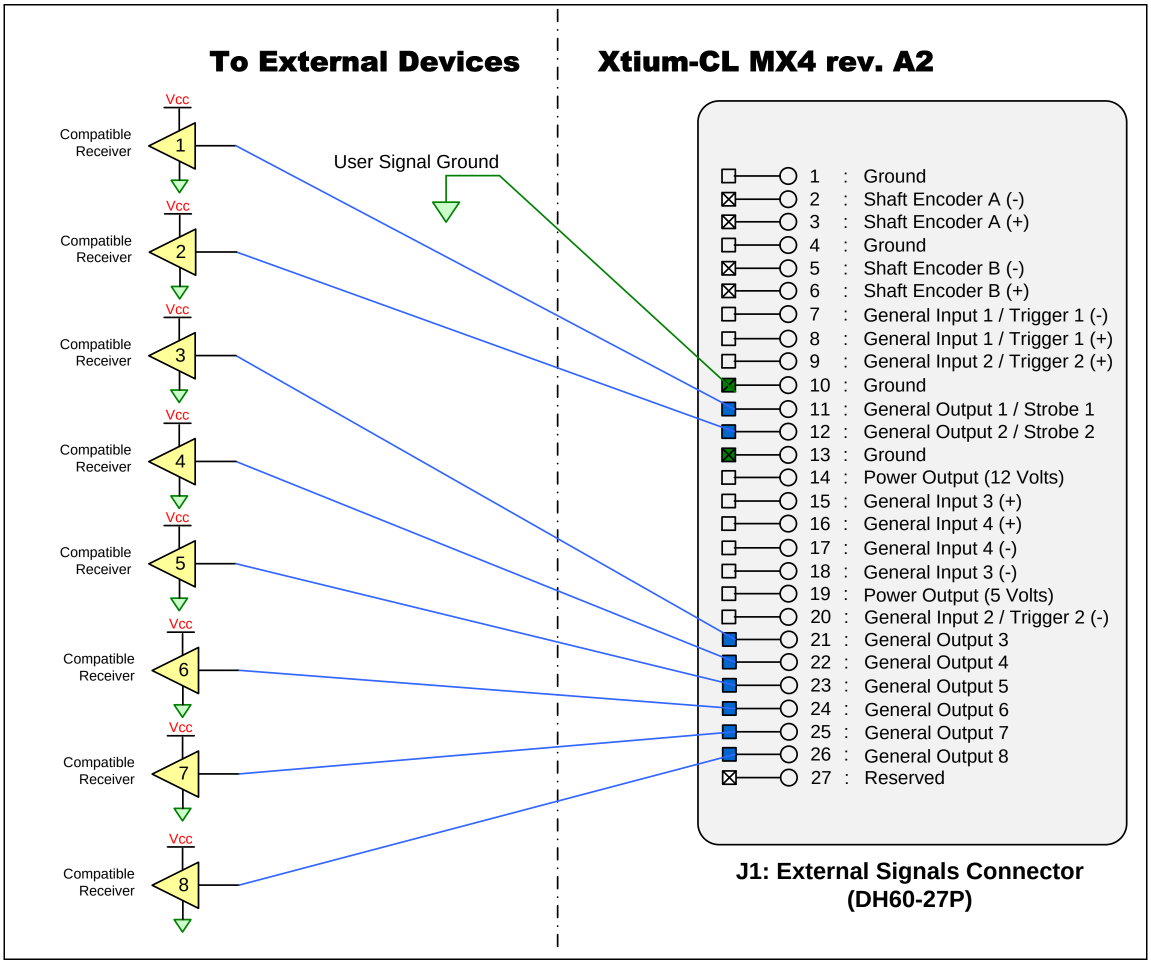


Figure 32:Rev A2/A3/Bx: Output Signals Connection Diagram

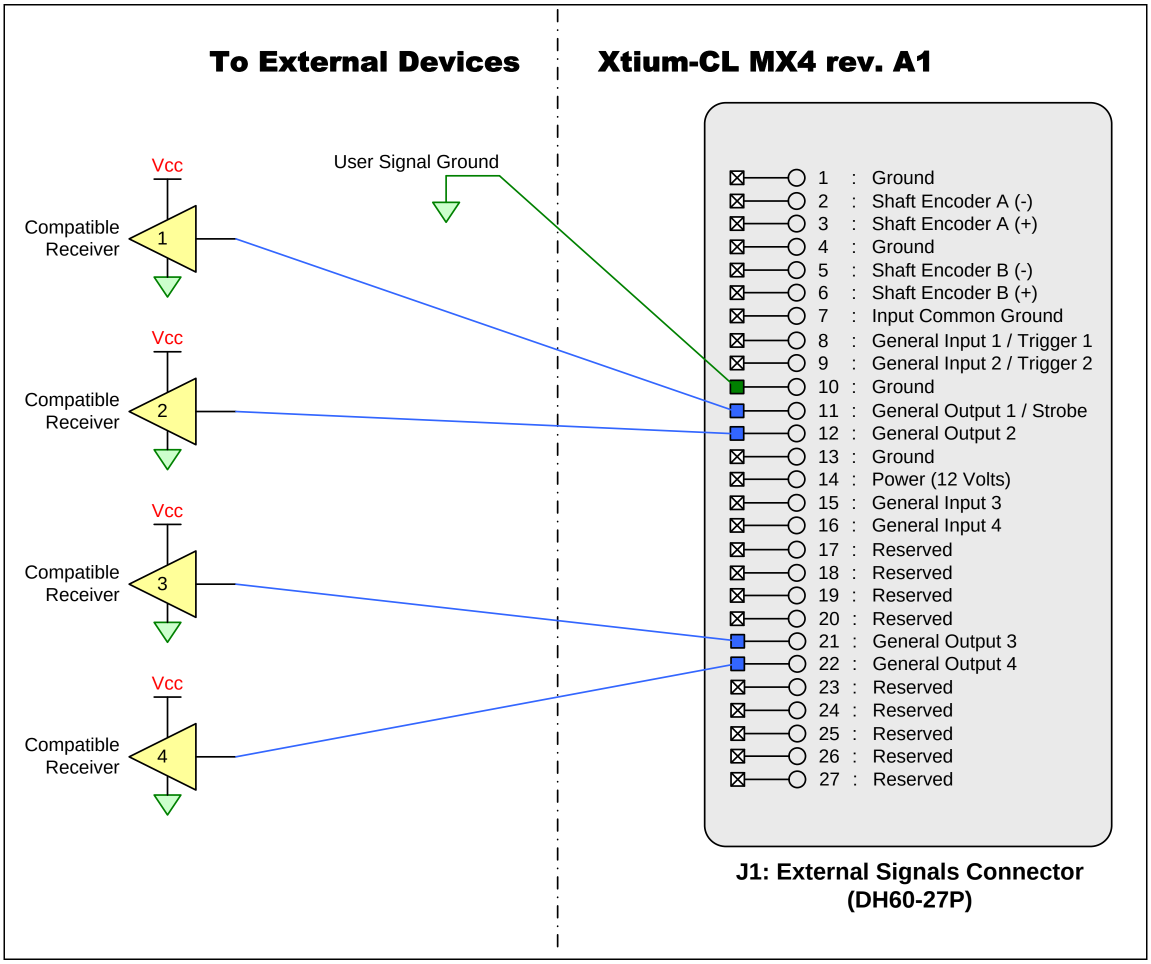


Figure 33:Rev A1: Output Signals Connection Diagram

External Receiver Electrical Requirements

- Xtium General Outputs are standard TTL logic levels.
- External receiver circuits must be compatible to TTL signals.

Input Level	Description	MIN	MAX
TTL	Input Voltage High (V_{IH})	2.0 V	–
	Input Voltage Low (V_{IL})	–	0.8 V

Note 3: RS-422/TTL Shaft Encoder Input Specifications

Dual Quadrature Shaft Encoder Inputs (phase A and phase B) connect to differential signals (RS-422), single ended signals, or TTL signals (Rev B Only). The figure below shows the simplified representation of these inputs.

	**WARNING:** When connecting shaft encoders to Xtium-CL MX4, make sure to connect a common ground between the shaft encoder and the frame grabber. See RED boxed connections in the diagram below. Failure to follow the described instructions could damage the board resulting in the shaft encoder functionality not working properly. Ensure that these grounding measures are followed when migrating from boards with opto-coupled shaft encoders (such as the Xcelera).

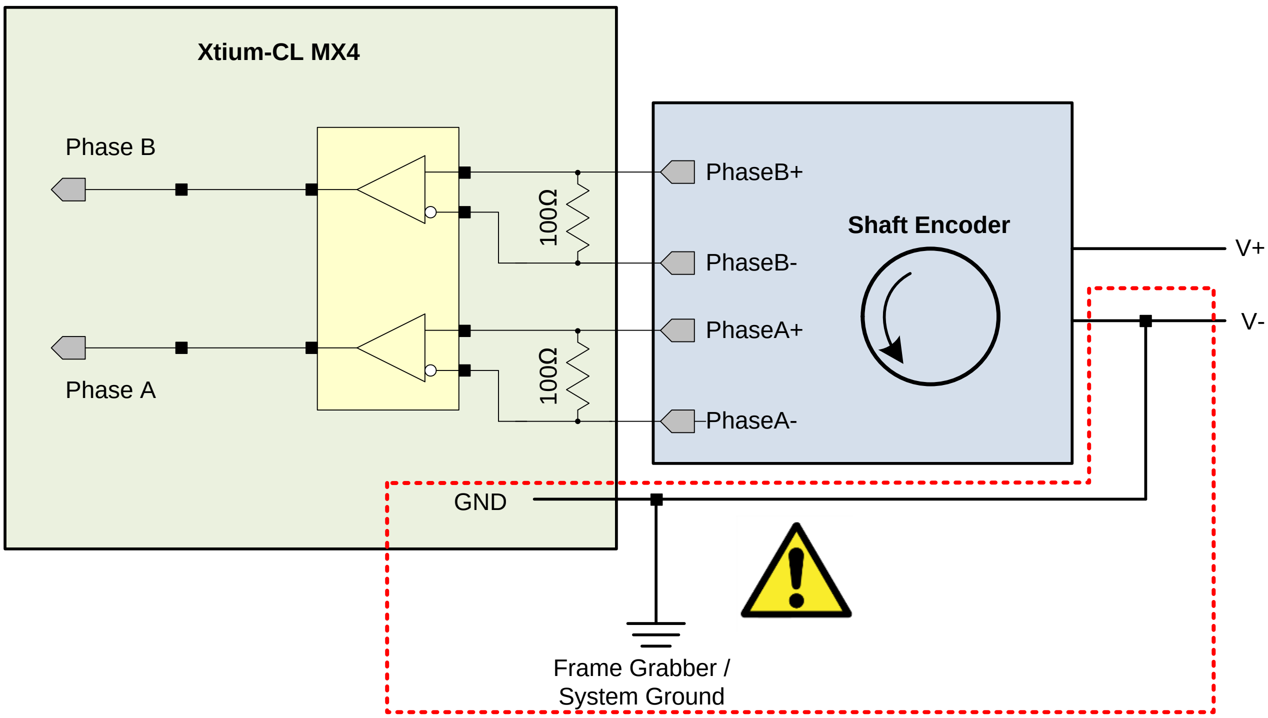


Figure 34: RS-422 Shaft Encoder Input Electrical Diagram

- The shaft encoder ground and the Xtium-CL MX4 computer system ground must be connected together.
- RS-422 Input Specifications:
  - Input signals must meet the following
    - Maximum differential input voltage is +/- 7V.
    - Minimum differential voltage level is +/- 200mV.
  - Both inputs have a 100-ohm differential resistor.

- TTL Input Specifications (Rev B Only):
  - Input signals must meet the following
    - Input voltage high minimum = 2V
    - Input voltage low maximum = 0.8V
  - Input Current Max = 5mA

- RS-422 differential line receiver used is am26lv32.
- Maximum input signal frequency is 10 MHz.
- The Xtium-CL provides ESD filtering on-board.
- See Line Trigger Source Selection for Line scan Applications for more information.
- Refer to Sapera parameters:
  CORACQ_PRM_SHAFT_ENCODER_ENABLE
  CORACQ_PRM_SHAFT_ENCODER_LEVEL
  CORACQ_PRM_SHAFT_ENCODER_DROP
  or refer to
  CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE
  CORACQ_PRM_EXT_LINE_TRIGGER_DETECTION
  CORACQ_PRM_EXT_LINE_TRIGGER_LEVEL (RS-422 or TTL)
  CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE
- See also *.cvi file entries:
  Shaft Encoder Enable, Shaft Encoder Pulse Drop,
  or see External Line Trigger Enable, External Line Trigger Detection, External Line Trigger Level, External Line Trigger Source.
- For single ended signals, connect a bias voltage to the RS-422 (-) input to ensure correct detection of the logic state of the signal connected to the RS-422 (+) input.
- For TTL signal (Rev B only), connect directly to RS-422 (+) input. See the following section for connection methods.

Note 3.1: Interfacing to an RS-422 Driver Output

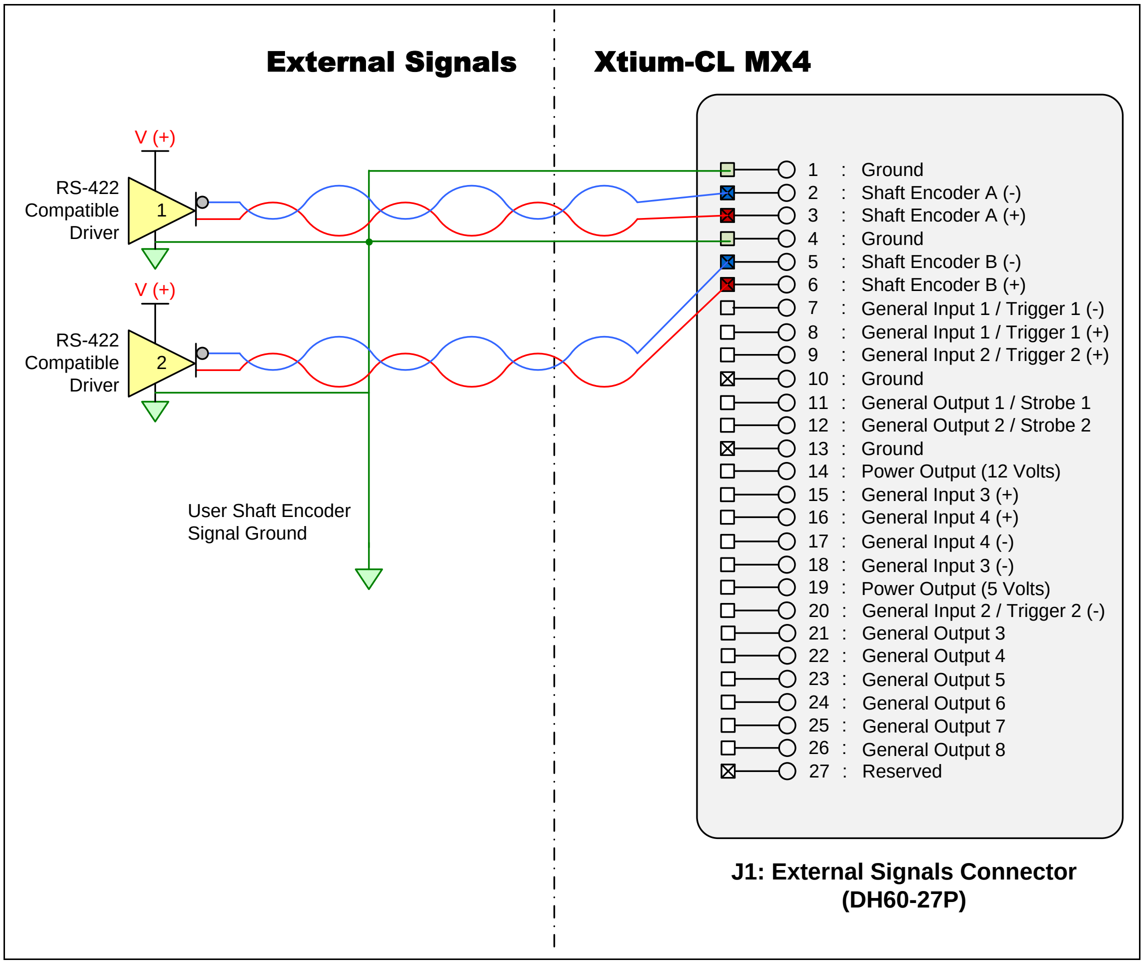


Figure 35:External RS-422 Signals Connection Diagram

Note 3.2: Interfacing to a TTL (also called Push-Pull) Output

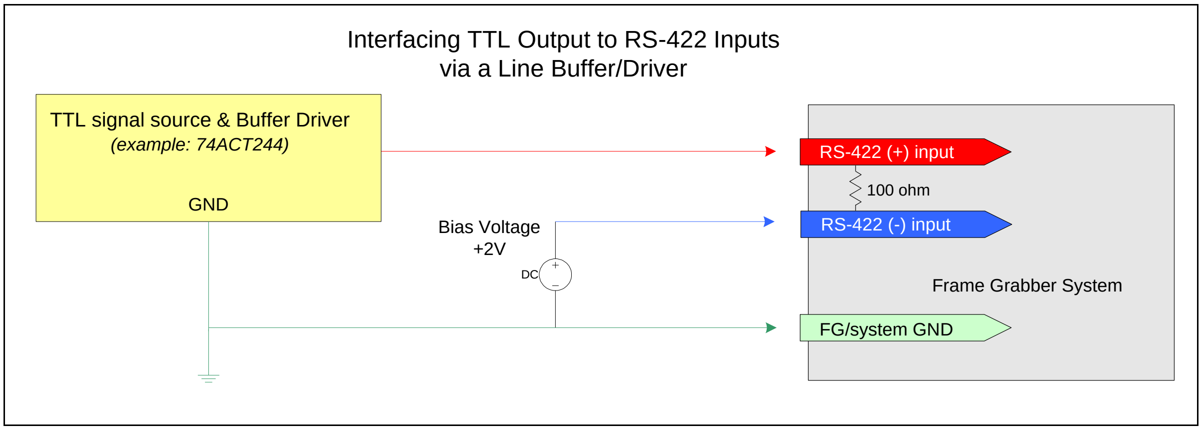


Figure 36: Interfacing TTL to RS-422 Shaft Encoder Inputs

- If necessary, a TTL input can be connected to the RS-422 input using a bias voltage; however, for board revision B, it is recommended to use the Shaft Encoder TTL mode described in Note 5)
- RS-422 (-) input is biased to a DC voltage of +2 volts.
- This guarantees that the TTL signal connected to the RS-422 (+) input will be detected as a logic high or low relative to the (-) input.
- The TTL shaft encoder ground, the bias voltage ground, and the Xtium-CL MX4 computer system ground must be connected together.
- DC voltage for the RS-422 (-) input can be generated by a resister voltage divider.
- Use a single battery cell if this is more suitable to your system.
- NOTE: User must select the Shaft Encoder RS-422 level when using this mode.

Note 3.3: Interfacing to a Line Driver (also called Open Emitter) Output

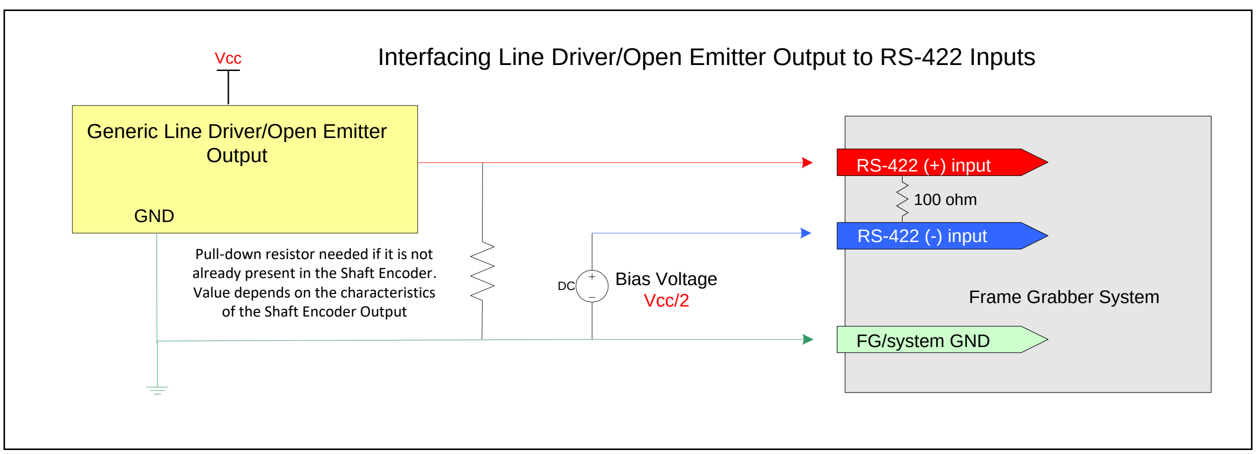


Figure 37: Interfacing to a Line Driver Output

- NOTE: User must select the Shaft Encoder RS-422 level when using this mode.

Note 3.4: Interfacing to an Open Collector Output

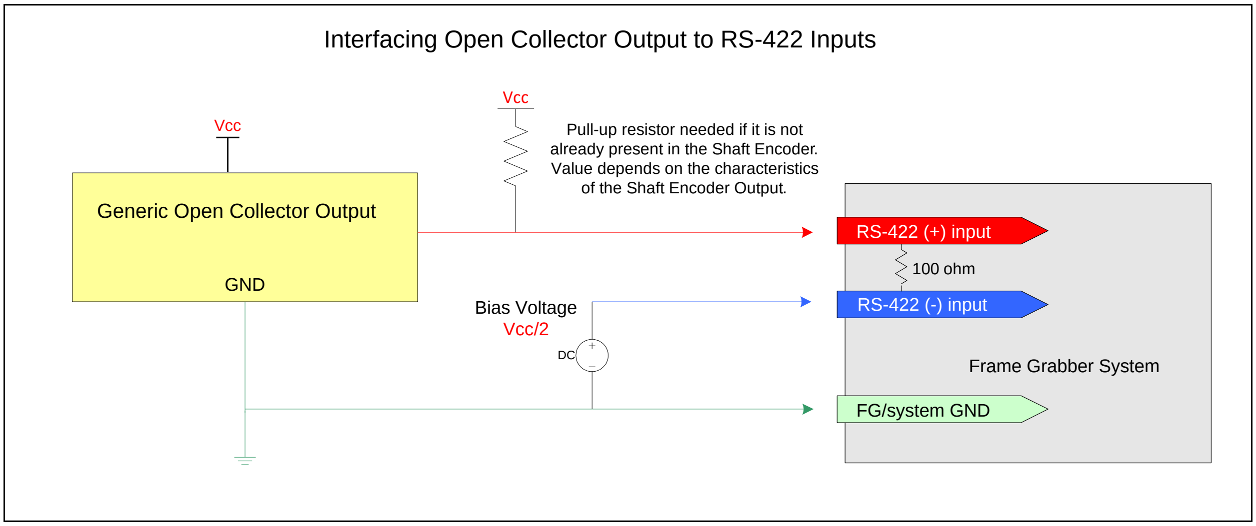


Figure 38: Interfacing to an Open Collector Output

NOTE: User must select the Shaft Encoder RS-422 level when using this mode

Note 3.5: Interfacing directly to a TTL (also called Push-Pull) Output (Rev B Only)

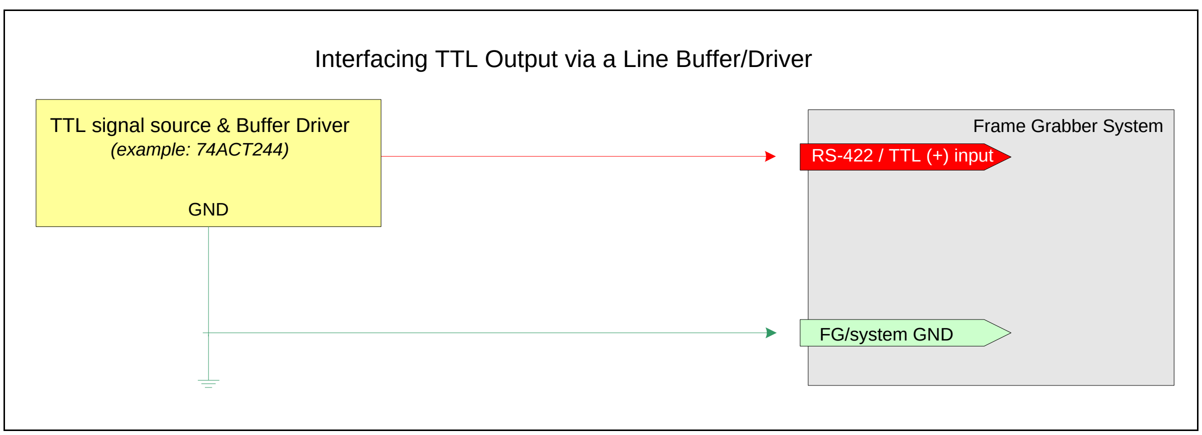


Figure 39: Interfacing TTL to TTL Shaft Encoder Inputs

- NOTE: User must select the Shaft Encoder TTL level when using this mode (CORACQ_PRM_SHAFT_ENCODER_LEVEL = CORACQ_VAL_LEVEL_TTL (0x1)).

J5: Multi-Board Sync / Bi-directional General I/Os

There are 8 bi-directional General I/Os that can be interconnected between multiple boards. These bi-directional I/Os can be read/written by Sapera application. Bi-directional General I/Os no.1 and no.2 also can also act as the multi-board sync I/Os.

The multi-board sync feature permits interconnecting multiple Xtium boards to synchronize acquisitions to one or two triggers or events. The trigger source origin can be either an external signal or a software control signal. The board sending the trigger(s) is the "Sync Master" board, while the one or more boards receiving the control signal(s) are "Sync Slaves".

Setup of the boards is done either by setting parameters via a Sapera application or by using CamExpert to configure two camera files (.ccf). For testing purposes, two instances of CamExpert (one for each board) can be run on the system where the frame grabbers are installed.

Hardware Preparation

- Interconnect two, three, or four Xtium boards via their J5 connector using the OR-YXCC-BSYNC20 cable (for 2 boards) or the OR-YXCC-BSYNC40 cable (see Board Sync Cable Assembly OR-YXCC-BSYNC40 for 3 or 4 boards).

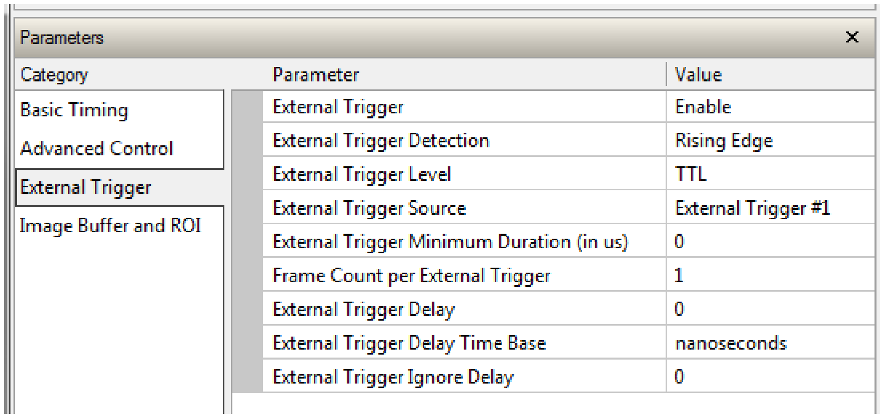
⚠	**Warning:** Multi-Board Sync / Bi-directional General I/Os are only for use with Teledyne DALSA frame grabbers within the same PC, otherwise electrical damage to boards can occur.

Configuration via Sapera Application Programming

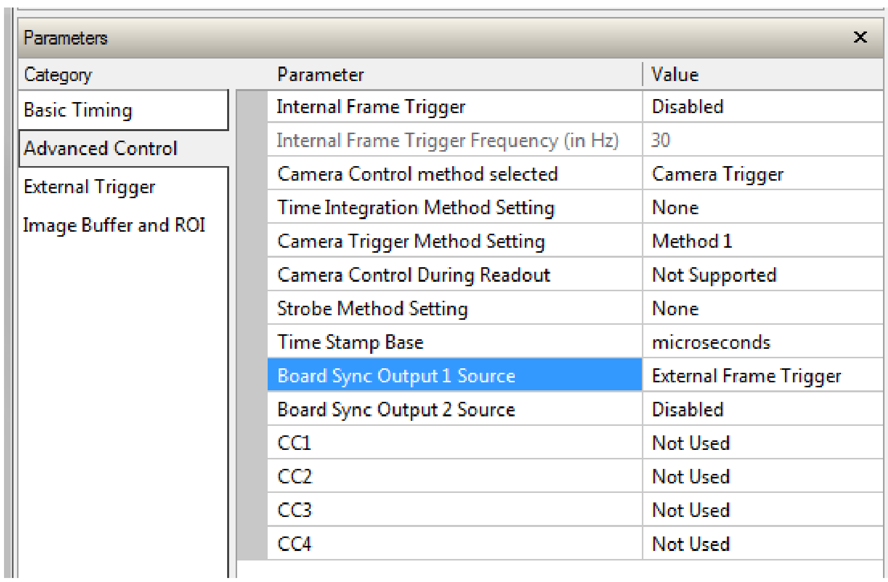
- **Sync Master Board** Software Setup: Choose one Xtium as "Sync Master". The Sapera parameter `CORACQ_PRM_BOARD_SYNC_OUTPUT1_SOURCE and/or CORACQ_PRM_BOARD_SYNC_OUTPUT2_SOURCE select the signal(s) to send to the "Sync Slave" boards.`
- Other "Sync Master" board parameters are set as for any external trigger application, such as External Trigger enable, detection, and level. See Sapera documentation for more details.
- **Sync Slave Board** Software Setup: The Sapera parameter CORACQ_PRM_EXT_TRIGGER_SOURCE and/or CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE are set to *Board Sync #1 or #2*.

Configuration via Sapera CamExpert

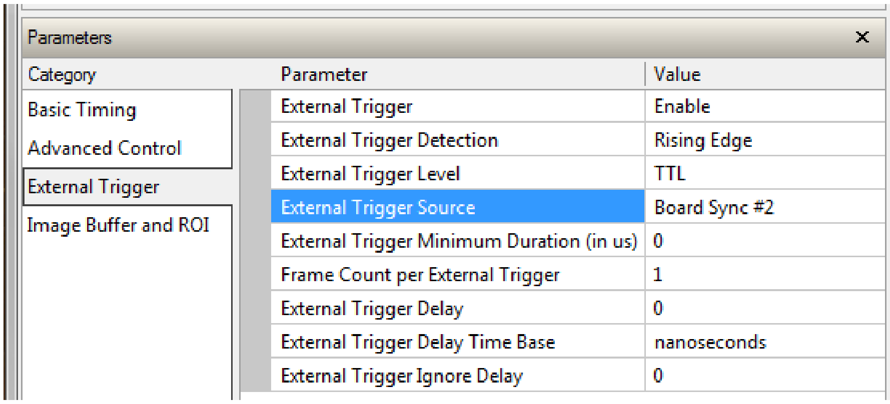
- Start the first instance of CamExpert and select one installed **Xtium board** to be the **sync master**. As shown in the following image, this board is configured to use an external trigger on input #1.



- The **Sync Master Xtium board** is also configured to output the external trigger on board sync #1, as shown in the following image.



- The **Sync Slave Xtium board** is configured to receive its trigger on the board sync signal. As an example the following image shows the Xtium board configured for an external sync on board sync #2.



- **Test Setup:** Start the acquisition on all slave boards. The acquisition process is now waiting for the control signal from the master board. Trigger master board acquisition and the acquisition start signal is sent to each slave board.

J7: Power Connector

DC Power Details

Warning: Never remove or install any hardware component with the computer power on. Never connect a power cable to J7 when the computer is powered on.

- Connect a computer 6-pin PCI Express power connector to J7 to supply DC power to the Camera Link connectors for PoCL operation and/or to supply power to connector J1. Older computers may need a power cable adapter (see Power Cable Assembly OR-YXCC-PWRY00).
- The 12 Volt can supply up to 8W of power to the cameras (4W per connector) and 6W to J1 or J4. Note that J1 and J4 have a 500 mA re-settable fuse on the board. If the fuse trips open, turn off the host computer power. When the computer is powered again, the fuse is automatically reset.

Differences between Rev A1, Rev A2/A3 and Rev B0

Board Revision	A1	A2/A3	B0
User Interface Outputs	4	8	8
Power on J1/J4	12V	5V and 12V	5V and 12V
User Interface Inputs	1 differential (LVDS/RS-422) /Single Ended + 3 Single Ended	4 differential (LVDS/RS-422), Single Ended	4 differential (LVDS/RS-422), Single Ended
Shaft Encoder Input	RS-422	RS-422	RS-422 or TTL

Cables & Accessories

The following cables and accessories are available for purchase. Contact sales at Teledyne DALSA.

DH40-27S Cable to Blunt End (OR-YXCC-27BE2M1, Rev B1)

Cable assembly consists of a 2000 mm (~6 ft.) blunt end cable to mate to Xtium external connector **J1**. Note: The applicable wiring color code table is included with the printed Product Notice shipped with the cable package — no other wiring table should be used.

Important: Cable part number OR-YXCC-27BE2M0 rev.3 is obsolete and should not be used with any Xtium series boards.

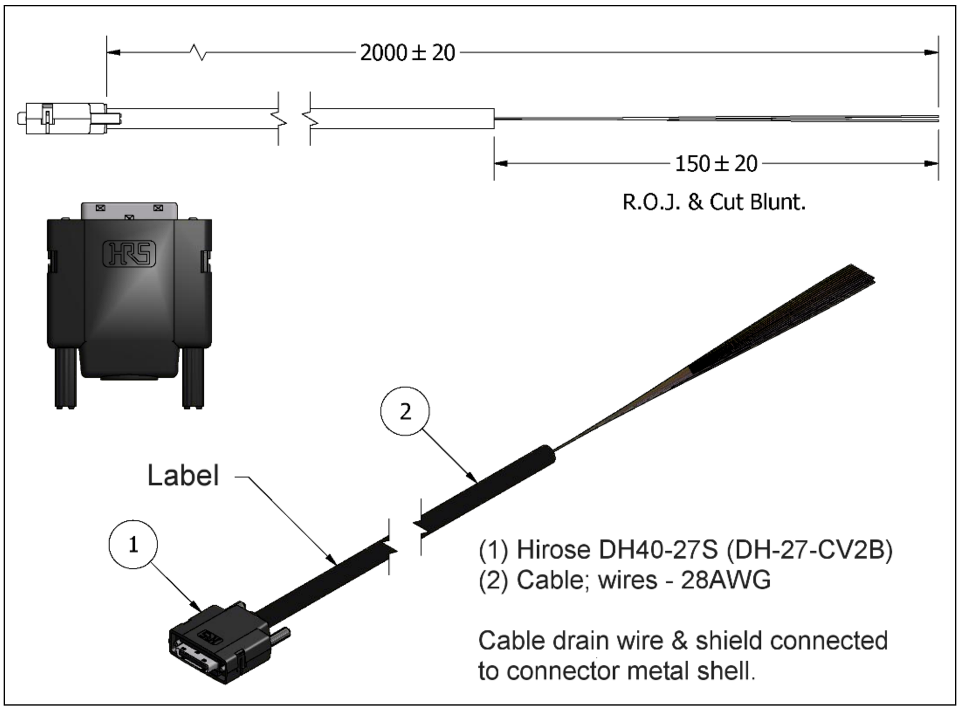


Figure 40: DH60-27P Cable No. OR-YXCC-27BE2M1 Detail

Figure 41: Photo of cable OR-YXCC-27BE2M1

DH40-27S Connector Kit for Custom Wiring

Teledyne DALSA makes available a kit comprised of the DH40-27S connector plus a screw lock housing package, for clients interested in assembling their own custom I/O cable. Order part number "OR-YXCC-H270000", (package as shown below).

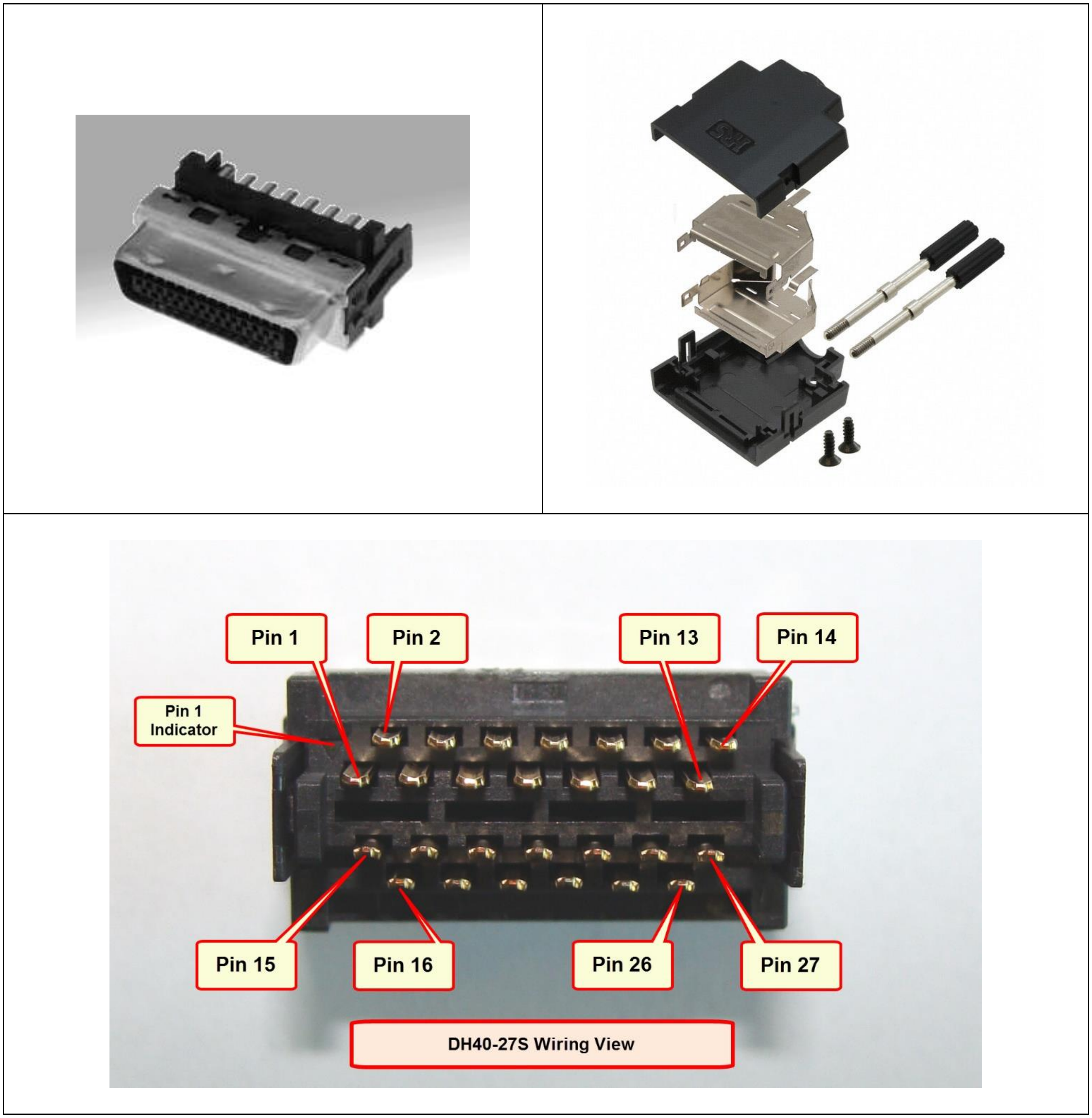


Figure 42: OR-YXCC-H270000 Custom Wiring Kit

Cable assemblies for I/O connector J4

Flat ribbon cables for connecting to J4 can be purchased from Teledyne DALSA or from third part suppliers, as described below.

Teledyne DALSA I/O Cable (part #OR-YXCC-TIOF120)

Contact Teledyne DALSA Sales to order the 12 inch (~30cm) I/O cable with connectors on both ends, as shown in the following picture.

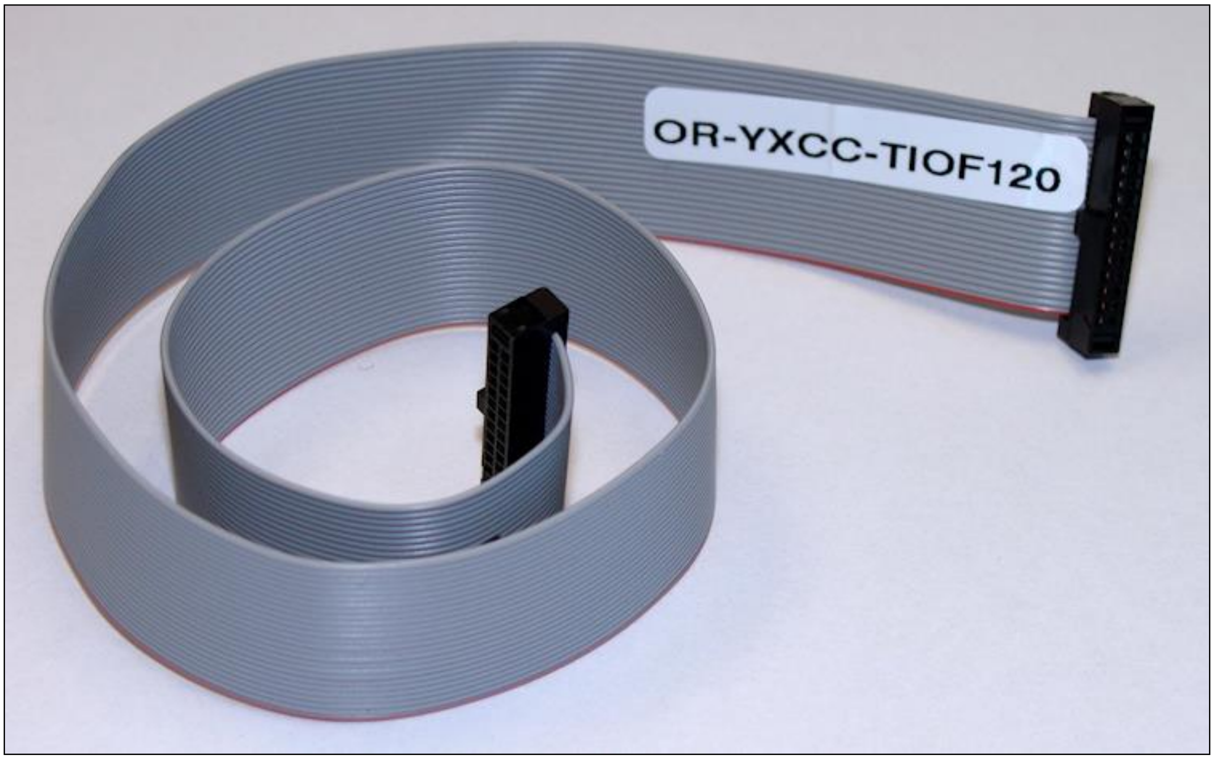


Figure 43: I/O Cable #OR-YXCC-TIOF120

Third Party I/O Cables for J4

Suggested third party cables are available from SAMTEC. Below are two examples:

- Connector to connector (FFSD-13-D-xx.xx-01-N)
- Connector to blunt end (FFSD-13-S-xx.xx-01-N)
- Note: xx.xx denotes length, where 06.00 is a 6 inch (~15 cm) length cable
- URL: http://cloud.samtec.com/catalog_english/FFSD.PDF

Board Sync Cable Assembly OR-YXCC-BSYNC40

This cable connects 3 to 4 Xtium boards for the board sync function as described in section. For a shorter 2 board cable, order cable assembly OR-YXCC-BSYNC20.

For a third party source of cables, see http://cloud.samtec.com/catalog_english/FFSD.PDF.

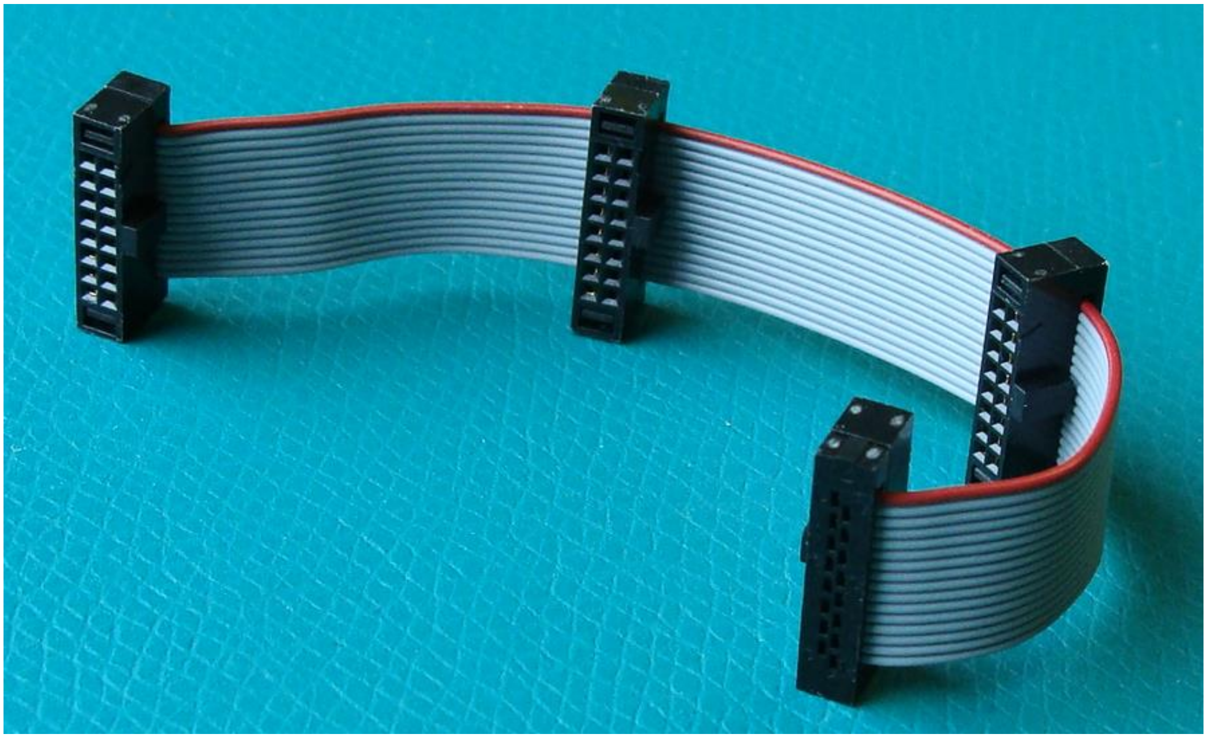


Figure 44: Photo of cable OR-YXCC-BSYNC40

Power Cable Assembly OR-YXCC-PWRY00

When the Xtium-CL MX4 supplies power to cameras via PoCL and/or when power is supplied to external devices via the J1/J4 I/O connector, PC power must be connected to the Xtium external power source connector (J7).

Recent computer power supplies provide multiple 6-pin power source connectors for PCI Express video cards, where one is connected to J7 on the Xtium-CL. But if the computer is an older model, this power supply adapter converts 2 standard 4-pin large power connectors to a 6-pin power connector.

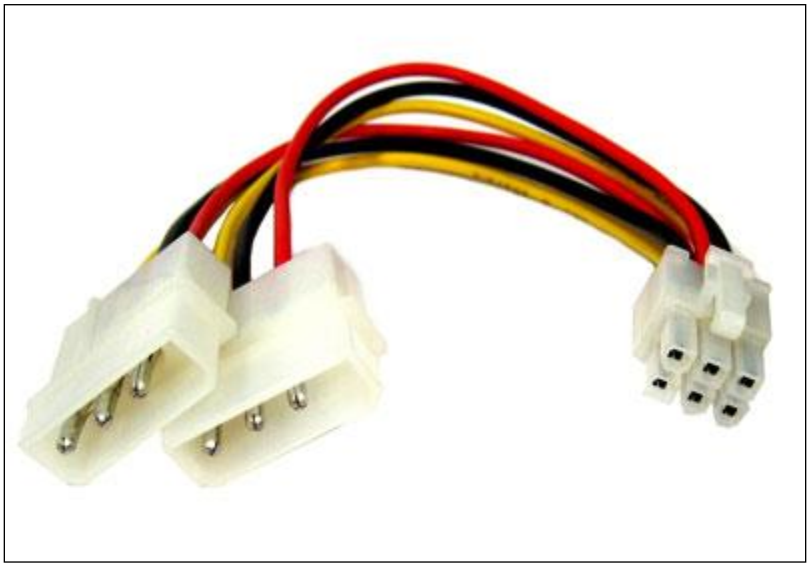


Figure 45: Photo of cable assembly OR-YXCC-PWRY00

This is an industry standard adapter cable which can be purchased from Teledyne DALSA.

Camera Link Interface

Camera Link Overview

Camera Link is a communication interface for vision applications developed as an extension of National Semiconductor's Channel Link technology. The advantages of the Camera Link interface are that it provides a standard digital camera connection specification, a standard data communication protocol, and simpler cabling between camera and frame grabber.

The Camera Link interface simplifies the usage of increasingly diverse cameras and high signal speeds without complex custom cabling. For additional information concerning Camera Link, see **http://en.wikipedia.org/wiki/Camera_Link**.

Rights and Trademarks

ℹ	Note: The following text is extracted from the Camera Link Specification 1.1 (January 2004).

The Automated Imaging Association (AIA), as sponsor of the Camera Link committee, owns the U.S. trademark registration for the Camera Link logo as a certification mark for the mutual benefit of the industry. The AIA will issue a license to any company, member or non-member, to use the Camera Link logo with any products that the company will self-certify to be compliant with the Camera Link standard. Licensed users of the Camera Link logo will not be required to credit the AIA with ownership of the registered mark.

Data Port Summary

The Camera Link interface has three configurations. A single Camera Link connection is limited to 28 bits requiring some cameras to have multiple connections or channels. The naming conventions for the three configurations are:

- Base: Single Channel Link interface, single cable connector
- Medium: Two Channel Link interface, two cable connectors
- Full: Three Channel Link interface, two cable connectors

A single Camera Link port is defined as having an 8-bit data word. The "Full" specification supports eight ports labeled as A to H.

Camera Signal Summary

Video Data

Four enable signals are defined as:

- FVAL Frame Valid (FVAL) is defined HIGH for valid lines
- LVAL Line Valid (LVAL) is defined HIGH for valid pixels
- DVAL Data Valid (DVAL) is defined HIGH when data is valid
- Spare A spare has been defined for future use

The camera provides the four enables on each Channel Link. All unused data bits must be set to a known value by the camera.

Camera Controls

Four LVDS pairs are reserved for general-purpose camera control, defined as camera inputs and frame grabber outputs.

- Camera Control 1 (CC1)
- Camera Control 2 (CC2)
- Camera Control 3 (CC3)
- Camera Control 4 (CC4)

> Note: the Xtium-CL MX4 by default implements the control lines as follows, (using Teledyne DALSA terminology):
>
> - (CC1) EXYNC
> - (CC2) PRIN
> - (CC3) FORWARD
> - (CC4) HIGH

Communication

Two LVDS pairs are allocated for asynchronous serial communication to and from the camera and frame grabber. Cameras and frame grabbers should support at least 9600 baud.

- SerTFG Differential pair with serial communications to the frame grabber
- SerTC Differential pair with serial communications to the camera

The serial interface protocol is one start bit, one stop bit, no parity, and no handshaking.

Camera Link Cable Manufacturer Contact Information

For additional information on Camera Link cables and their specifications, visit the following web sites:

For Information contact: *(see their web site for worldwide offices)*	Alysium-Tech GmbH Andernacher Strasse 31b 90411 Nuremberg Phone: +49 [0] 911 93 78 78 0 Fax: +49 [0] 911 93 78 78 93 https://www.alysium.com/
For Information contact: *(see their web site for worldwide offices)*	Components Express, Inc. (CEI) 10330 Argonne Woods Drive, Suite 100 Woodridge, IL 60517-4995 Phone: 630-257-0605 / 800.578.6695 (outside Illinois) Fax: 630-257-0603 http://www.componentsexpress.com/

Appendix A: Silent Installation

Both Sapera LT and the Xtium-CL MX4 driver installations share the same installer technology. When the installations of Teledyne DALSA products are embedded within a third party's product installation, the mode can either have user interaction or be completely silent. The following installation mode descriptions apply to both Sapera and the hardware driver.

	Note: You must reboot after the installation of Sapera LT. However, to streamline the installation process, Sapera LT can be installed without rebooting before installing the board hardware device drivers. The installations then complete with a single final system reboot.

Perform Teledyne DALSA embedded installations in either of these two ways:

- **Normal Mode**
  The default mode is interactive. This is identical to running the setup.exe program manually from Windows (either run from Windows Explorer or the Windows command line).
- **Silent Mode**
  This mode requires no user interaction. A preconfigured "response" file provides the user input. The installer displays nothing.

Silent Mode Installation

A Silent Mode installation is recommended when integrating Teledyne DALSA products into your software installation. The silent installation mode allows the device driver installation to proceed without the need for mouse clicks or other input from a user.

Preparing a Silent Mode Installation requires two steps:

- Prepare the response file, which emulates a user.
- Invoke the device driver installer with command options to use the prepared response file.

Creating a Response File

Create the installer response file by performing a device driver installation with a command line switch "-r". The response file is automatically named **setup.iss** and is saved in the \windows folder. If a specific directory is desired, the switch –f1 is used.

As an example, to save a response file in the same directory as the installation executable of the Xtium-CL MX4, the command line would be:

```
Xtium-CL_MX4_1.00.00.0000 –r –f1".\setup.iss"
```

Running a Silent Mode Installation

A device driver silent installation, whether done alone or within a larger software installation requires the device driver executable and the generated response file **setup.iss**.

Execute the device driver installer with the following command line:

```
Xtium-CL_MX4_1.00.00.0000 -s -f1".\setup.iss"
```

Where the **–s** switch specifies the silent mode and the **–f1** switch specifies the location of the response file. In this example, the switch –f1".\setup.iss" specifies that the **setup.iss** file be in the same folder as the device driver installer.

	Note: On Windows 7, 8 and 10, the Windows Security dialog box will appear unless one has already notified Windows to 'Always trust software from "Teledyne DALSA Inc." during a previous installation of a driver.

Silent Mode Uninstall

Similar to a silent installation, a response file must be prepared first as follows.

Creating a Response File

The installer response file is created by performing a device driver un-installation with a command line switch "-r". The response file is automatically named **`setup_uninstall.iss`** which is saved in the \windows folder. If a specific directory is desired, the switch "–f1" is used.

As an example, to save a response file in the same directory as the installation executable of the Xtium-CL MX4, the command line would be:

```
Xtium-CL_MX4_1.00.00.0000 –r –f1".\setup_uninstall.iss"
```

Running a Silent Mode Uninstall

Similar to the device driver silent mode installation, the un-installation requires the device driver executable and the generated response file **`setup.iss`**.

Execute the device driver installer with the following command line:

```
Xtium-CL_MX4_1.00.00.0000 -s -f1".\setup_uninstall.iss"
```

Where the **–s** switch specifies the silent mode and the **–f1** switch specifies the location of the response file. In this example, the switch –f1".\setup_uninstall.iss" specifies that the **`setup_uninstall.iss`** file be in the same folder as the device driver installer.

Silent Mode Installation Return Code

A silent mode installation creates a file "corinstall.ini" in the Windows directory. A section called [SetupResult] contains the 'status' of the installation. A value of 1 indicates that the installation has started and a value of 2 indicates that the installation has terminated.

A silent mode installation also creates a log file "setup.log" which by default is created in the same directory and with the same name (except for the extension) as the response file. The /f2 option enables you to specify an alternative log file location and file name, as in `Setup.exe /s /f2"C:\Setup.log"`.

The "setup.log" file contains three sections. The first section, [InstallShield Silent], identifies the version of InstallShield used in the silent installation. It also identifies the file as a log file. The second section, [Application], identifies the installed application name, version, and the company name. The third section, [ResponseResult], contains the 'ResultCode' indicating whether the silent installation succeeded. A value of 0 means the installation was successful.

Installation Setup with CorAppLauncher.exe

The installation setup can be run with the CorAppLauncher.exe tool provided with the driver.

- Install the board driver and get CorAppLauncher.exe from the \bin directory of the installation.
- When running the installation, CorAppLauncher.exe will return only when the installation is finished.
- When run from within a batch file, obtain the installation exit code from the ERRORLEVEL value.
- The arguments to CorAppLauncher.exe are
  -l: Launch application
  -f: Application to launch. Specify a fully qualified path.

As an example:

- CorAppLauncher –l –f"c:\driver_install\Xtium-cl_MX4_1.00.00.0000.exe"
- IF %ERRORLEVEL% NEQ 0 goto launch error

Note: There is a 32-bit and 64-bit version of CorAppLauncher.exe. When installing the driver, only the version related to the OS is installed. However, the 32-bit version is usable on either 32-bit or 64-bit Windows.

Custom Driver Installation using install.ini

Customize the driver installation by parameters defined in the file "install.ini". By using this file, the user can:

- Select the user default configuration.
- Select different configurations for systems with multiple boards.
- Assign a standard Serial COM port to board.

Creating the install.ini File

- Install the driver in the target computer. All Xtium-CL MX4 boards required in the system must be installed.
- Configure each board's acquisition firmware using the Teledyne DALSA Device Manager tool (see Device Manager – Board Viewer).
- If a standard Serial COM port is required for any board, use the Sapera Configuration tool (see COM Port Assignment).
- When each board setup is complete, using the Teledyne DALSA Device Manager tool, click on the Save Config File button. This will create the "install.ini" file.

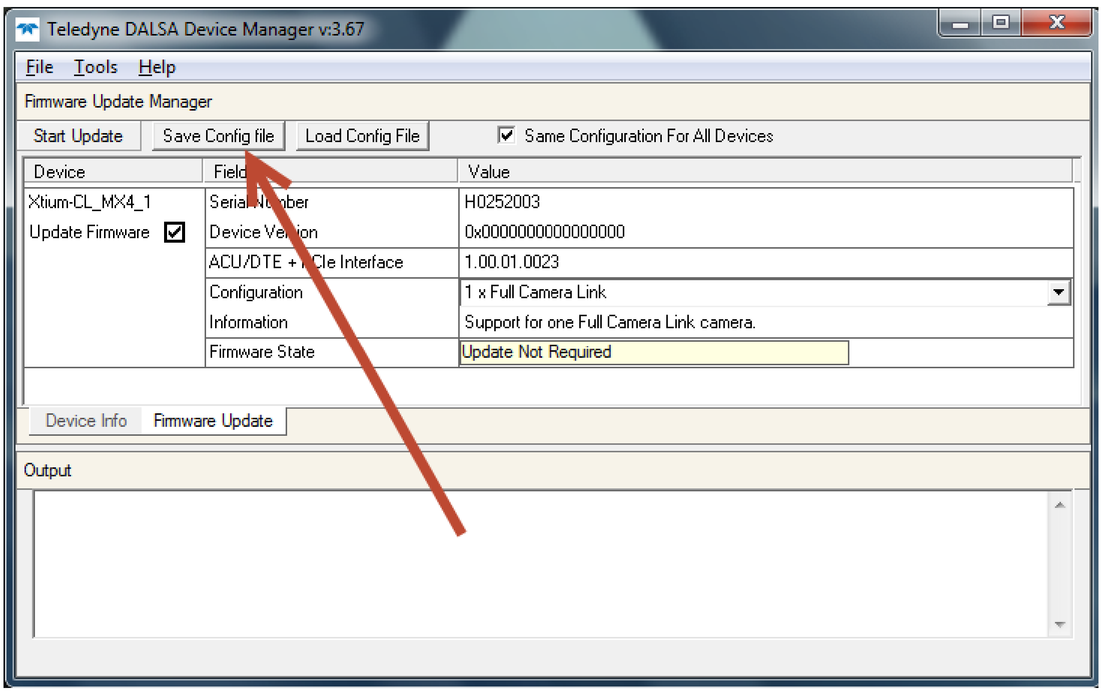


Figure 46: Create an install.ini File

Run the Installation using install.ini

Copy the install.ini file into the same directory as the setup installation file. Run the setup installation as normal. The installation will automatically check for an install.ini file and if found, use the configuration defined in it.

Appendix B: Troubleshooting Installation Problems

Overview

The Xtium-CL MX4 (and the Xtium family of products) is tested by Teledyne DALSA in a variety of computers. Although unlikely, installation problems may occur due to the constant changing nature of computer equipment and operating systems. This section describes what the user can verify to determine the problem or the checks to make before contacting Teledyne DALSA Technical Support.

If you require help and need to contact Teledyne DALSA Technical Support, make detailed notes on your installation and/or test results for our Technical Support to review. Importantly, please be clear about the problem being an installation issue or functional issue, and which of the following test tools were used.

Problem Type Summary

Xtium-CL MX4 problems are either installation types where the board hardware is not recognized on the PCIe bus (i.e. trained), or function errors due to camera connections or bandwidth issues. The following links jump to various topics in this troubleshooting section.

First Step: Check the Status LED

Status LED D1 should be **GREEN** or flashing **GREEN** just after boot up. If it remains flashing **RED**, the board firmware did not load correctly. If LED D1 is **BLUE** or flashing **BLUE**, the board is running from the safe mode load.

Camera Link status is indicated by the two LEDs (D3, D4) mounted next to each Camera Link connector. These LEDs show the presence of the pixel clock and an active acquisition.

The complete status LED descriptions are available in the technical reference section (see Status LED Functional Description.

Possible Installation Problems

- **Hardware PCI bus conflict:** When a new installation produces PCI bus error messages or the board driver does not install, it is important to verify that there are no conflicts with other PCI or system devices already installed. Use the Teledyne DALSA PCI Diagnostic tool as described in Checking for PCI Bus Conflicts. Also verify the installation via the Windows Device Manager.
- **BSOD (blue screen) following a board reset:** After programming the board with different firmware, the computer displays the BSOD when the board is reset (see BSOD (blue screen) Following a Board Reset).
- **Verify Sapera and Board drivers:** If there are errors when running applications, confirm that all Sapera and board drivers are running. See Sapera and Hardware Windows Drivers for details. In addition, Teledyne DALSA technical support will ask for the log file of messages by Teledyne DALSA drivers. Follow the instructions describe in Teledyne DALSA Log Viewer.
- **Firmware update error:** There was an error during the Xtium-CL MX4 firmware update procedure. The user can usually easily correct this. Follow the instructions Recovering from a Firmware Update Error.
- Installation went well but the board doesn't work or stopped working. Review these steps described in Symptoms: CamExpert Detects no Boards.
- **Using Windows 8/10 Fast Boot option:** When adding, removing, or moving boards while the PC is shutdown with the Windows Fast Boot option activated, it is possible that the boards don’t get mapped properly on the next reboot of the computer. The driver will detect such a situation and the Device Manager launched at startup will display a message indicating that a reboot is required.

Possible Functional Problems

- **Driver Information:** Use the Teledyne DALSA device manager program to view information about the installed Xtium-CL MX4 board and driver. See Driver Information via the Device Manager Program.
- **On-Board Image Memory Requirements:** The Xtium-CL MX4 on-board memory can provide two frame buffers large enough for most imaging situations. See On-board Image Memory Requirements for Acquisitions for details on the on board memory and possible limitations.
- **Inconsistent Acquisition Issues:** Acquisition or functional problems that might be random or become frequent might point to a board temperature issue or hardware voltage instabilities. Use the Board Hardware Diagnostic Tool to monitor and report these parameters, as described in section Diagnostic Tool Overview.

Sometimes the problem symptoms are not the result of an installation issue but due to other system issues. Review the sections described below for solutions to various Xtium-CL MX4 functional problems.

- Symptoms: Xtium-CL MX4 Does Not Grab
- Symptoms: Card grabs black
- Symptoms: Card acquisition bandwidth is less than expected

Troubleshooting Procedures

The following sections provide information and solutions to possible Xtium-CL MX4 installation and functional problems. The previous section of this manual summarizes these topics.

Diagnostic Tool Overview

The Xtium-CL MX4 Board Diagnostic Tool provides a quick method to see board status and health. It additionally provides live monitoring of FPGA temperature and voltages, which may help in identifying problems.

Diagnostic Tool Main Window

The main window provides a comprehensive view of the installed Xtium board. Toolbar buttons execute the board self test function and open a FPGA live status window.

Important parameters include the PCI Express bus transfer supported by the host computer and the internal Xtium FPGA temperature. The bus transfer defines the maximum data rate possible in the computer, while an excessive FPGA temperature may explain erratic acquisitions due to poor computer ventilation.

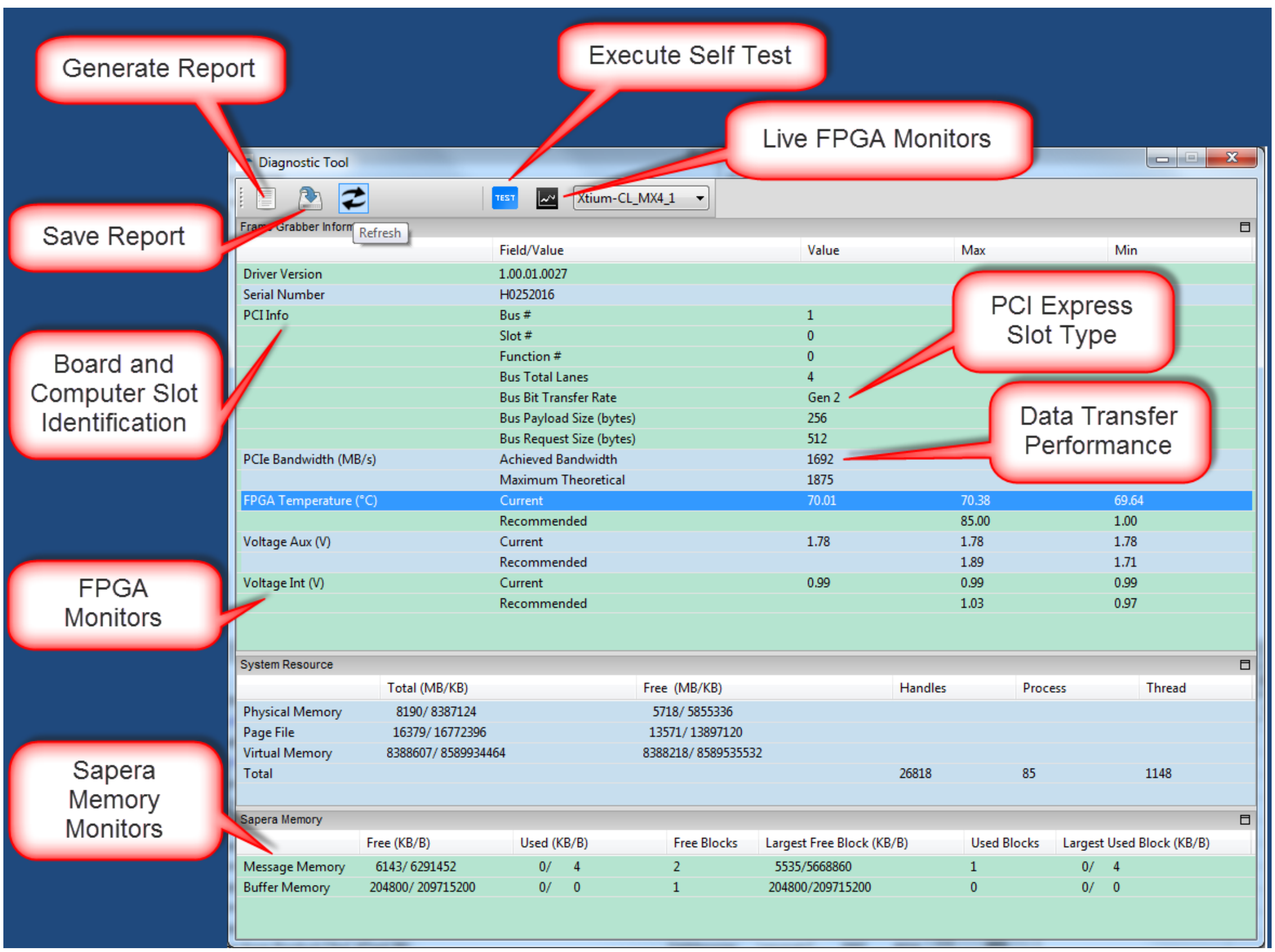


Figure 47: Diagnostic Tool Main Window

	Note: when the Xtium-CL MX4 firmware is configured for dual acquisition (2 x Base Camera Link), the PCIe bus transfer is divided equally between the two inputs. The Diagnostic Tool displays the PCIe bandwidth statistics for one input (for example, the total maximum bandwidth for each input is half the PCIe bus capability).

Diagnostic Tool Self Test Window

Click the Start button to initiate the board memory self test sequence. A healthy board will pass all memory test patterns.

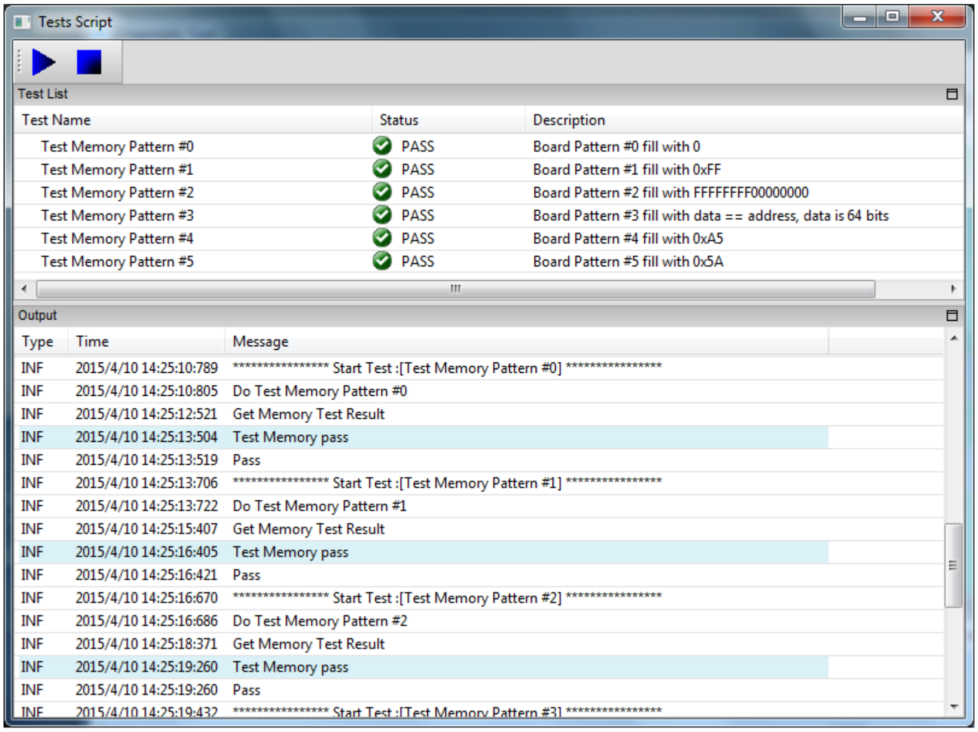


Figure 48: Diagnostic Tool Self Test Window

Diagnostic Tool Live Monitoring Window

The three FPGA parameters listed on the main window can also be monitored in real time. Choosing a parameter puts that graph at the top where the user can select the time unit and time range. Clicking the Output button will open a window displaying any error messages associated with that parameter.

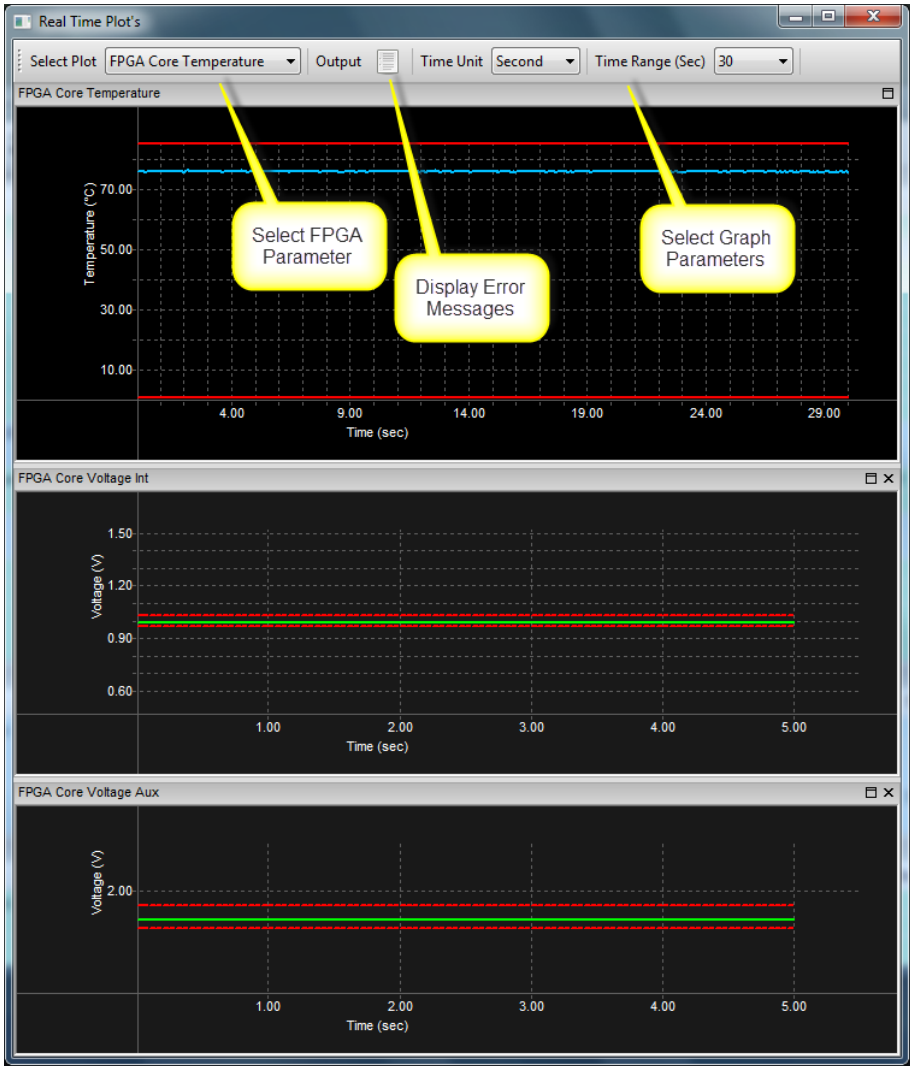


Figure 49: PCI Diagnostic Tool Live Monitoring Window

Checking for PCI Bus Conflicts

One of the first items to check when there is a problem with any PCI board is to examine the system PCI configuration and ensure that there are no conflicts with other PCI or system devices. The *PCI Diagnostic* program (**cpcidiag.exe**) allows examination of the PCI configuration registers and can save this information to a text file. Run the program via the Windows Start Menu shortcut **Start • Programs • Teledyne DALSA • Sapera LT • Tools • PCI Diagnostics**.

As shown in the following screen image, use the first drop menu to select the PCI device to examine. Select the device from Teledyne DALSA. Note the bus and slot number of the installed board (this will be unique for each system unless systems are setup identically). Click on the **Diagnostic** button to view an analysis of the system PCI configuration space.

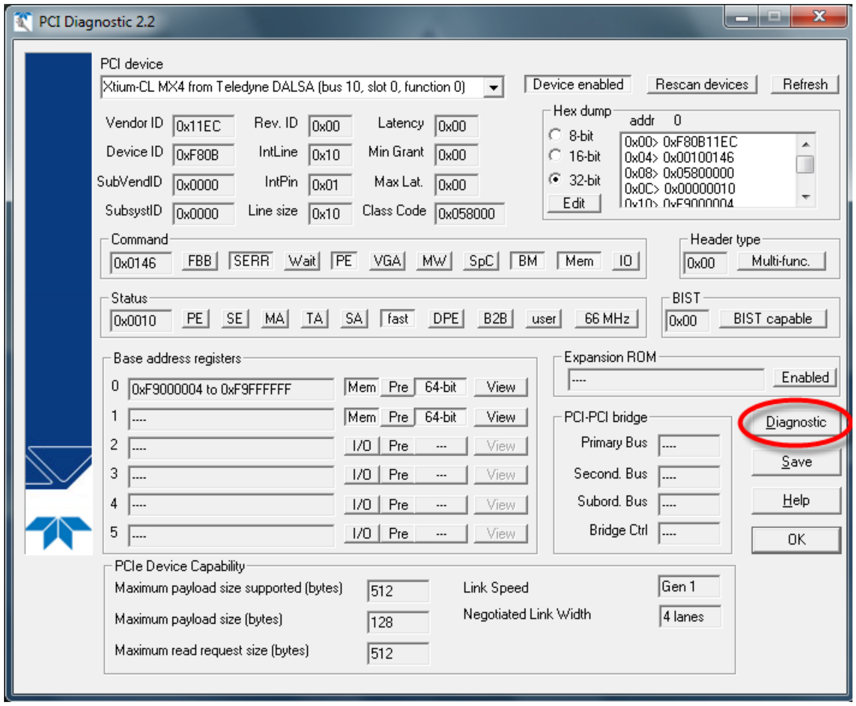


Figure 50: PCI Diagnostic Program

Clicking on the **Diagnostic** button opens a new window with the diagnostic report. From the PCI Bus Number drop menu, select the bus number that the Xtium-CL MX4 is installed in—in this example the slot is bus 10.

The window now shows the I/O and memory ranges used by each device on the selected PCI bus. The information display box will detail any PCI conflicts. If there is a problem, click on the **Save** button. A file named '**pcidiag.txt**' is created (in the Sapera\bin directory) with a dump of the PCI configuration registers. Email this file when requested by the Teledyne DALSA Technical Support group along with a full description of your computer.

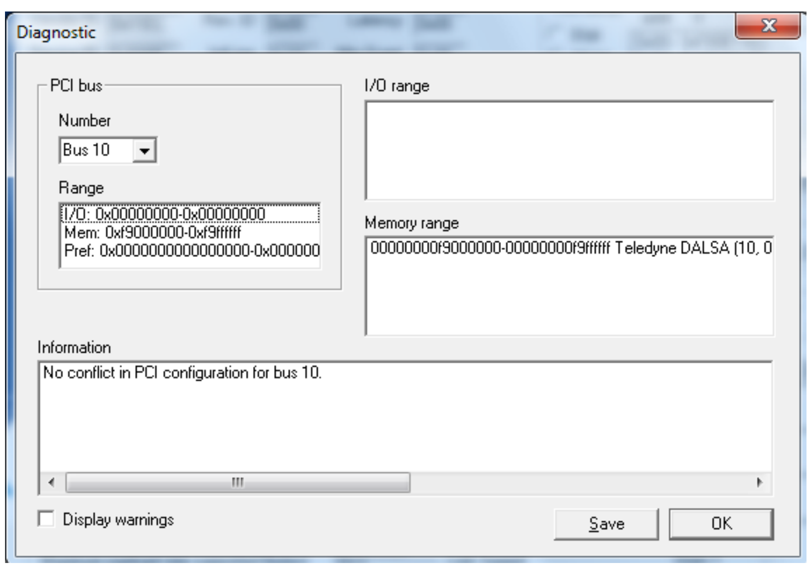


Figure 51: PCI Diagnostic Program – PCI bus info

Windows Device Manager

An alternative method to confirm the installation of the Xtium-CL MX4 board and driver is to use the Windows Device manager tool. Use the Start Menu shortcut **Start • Control Panel • System • Device Manager**. As shown in the following screen images, look for *Xtium-CL MX4* board under “Imaging Devices”. Double-click and look at the device status. You should see “This device is working properly.” Go to “Resources” tab and make certain that the device has an interrupt assigned to it, without conflicts.

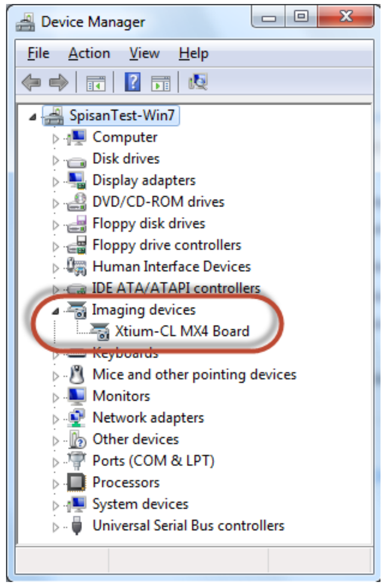


Figure 52: Using Windows Device Manager

BSOD (blue screen) Following a Board Reset

Teledyne DALSA engineering has identified cases where a PC will falsely report a hardware malfunction when the Xtium-CL MX4 board is reset. The symptoms will be a Windows blue screen or PC that freezes following a board reset.

The 1st solution to this problem is to use the Xtium-CL MX4 driver 1.00 or higher along with Sapera LT 7.40 or higher. If this still does not resolve the issue, then uninstall the driver and reinstall it using the switch “/cr”, which will not reset the board at the end of the installation but requires a reboot of the computer instead.

- **Example**: Xtium-CL_MX4_1.00.00.0000.exe /cr

Sapera and Hardware Windows Drivers

Any problem seen after installation, such as an error message running CamExpert, first make certain the appropriate Teledyne DALSA drivers have started successfully during the boot sequence. Example, click on the **Start • Programs • Accessories • System Tools • System Information • Software Environment** and click on **System Drivers**. Make certain the following drivers have started for the **Xtium-CL MX4**.

Device	**Description**	**Type**	**Started**
CorXtiumCLMX4	Xtium-CL MX4 messaging	Kernel Driver	Yes
CorLog	Sapera Log viewer	Kernel Driver	Yes
CorMem	Sapera Memory manager	Kernel Driver	Yes
CorPci	Sapera PCI configuration	Kernel Driver	Yes
CorSerial	Sapera Serial Port manager	Kernel Driver	Yes

Teledyne DALSA Technical Support may request that you check the status of these drivers as part of the troubleshooting process.

Recovering from a Firmware Update Error

This procedure is required if any failure occurred while updating the Xtium-CL MX4 firmware on installation or during a manual firmware upgrade. If on the case the board has corrupted firmware, any Sapera application such as CamExpert or the grab demo program will not find an installed board to control.

Possible reasons for firmware loading errors or corruption are:

- Computer system mains power failure or deep brown-out
- PCI bus or checksum errors
- PCI bus timeout conditions due to other devices
- User forcing a partial firmware upload using an invalid firmware source file

When the Xtium-CL MX4 firmware is corrupted, the board will automatically run from the Safe load after a board and/or PC reset.

***Solution*:** Update the board using the standard method described in section Firmware Update: Automatic ModeFirmware Update: Automatic Mode

Driver Information via the Device Manager Program

The Device Manager program provides a convenient method of collecting information about the installed Xtium-CL MX4. System information such as operating system, computer CPU, system memory, PCI configuration space, plus Xtium-CL MX4 firmware information is displayed or written to a text file (default file name – BoardInfo.txt). Note that this program also manually uploads firmware to the Xtium-CL MX4 (described elsewhere in this manual).

Execute the program via the Windows Start Menu shortcut **Start • Programs • Teledyne DALSA • Xtium-CL MX4 Device Driver • Device Manager**. If the Device Manager Program does not run, it will exit with a board was not found message. Possible reasons for an error are:

- Board is not in the computer
- Board driver did not start or was terminated
- PCI conflict after some other device was installed

Information Window

The following figure shows the Device Manager Information screen. Click to highlight one of the board components and its information shows in the right hand window, as described below.

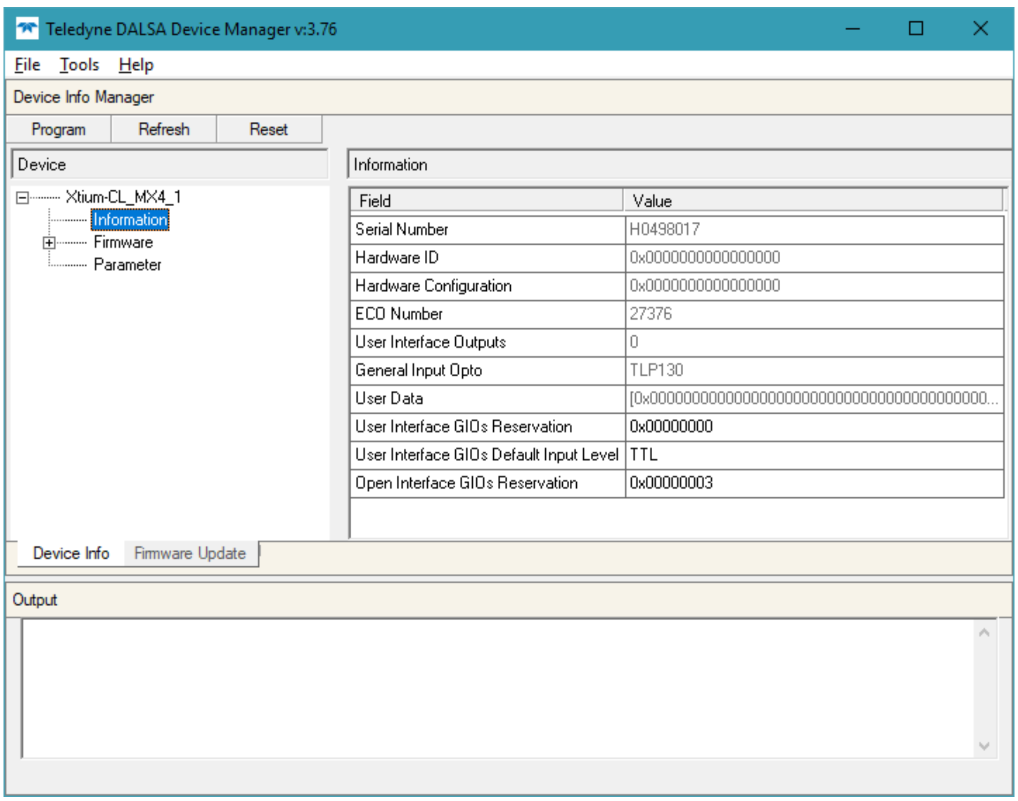


Figure 53: Board Firmware Version

- Select **Information** to display identification and information stored in the Xtium-CL MX4 firmware.
- Select **Firmware** to display version information for the firmware components.
- Select one of the firmware components to load *custom* firmware when supplied by Teledyne DALSA engineering for a future feature.
- Click on **File • Save Device Info** to save all information to a text file. Email this file when requested by Technical Support.

Teledyne DALSA Log Viewer

The third step in the verification process is to save in a text file the information collected by the Log Viewer program. Run the program via the Windows Start Menu shortcut **Start • Programs • Teledyne DALSA • Sapera LT • Tools • Log Viewer**.

The Log Viewer lists information about the installed Teledyne DALSA drivers. Click on File • Save and you will be prompted for a text file name to save the Log Viewer contents. Email this text file to Teledyne DALSA Technical Support when requested or as part of your initial contact email.

On-board Image Memory Requirements for Acquisitions

The Xtium-CL MX4 by default will allocate the maximum number of buffers that can fit in on-board memory based on the size of the acquired image before cropping, to a maximum of 65535 buffers.

Note that an application can change the default number of on-board frame buffers using the Sapera LT API. Usually two buffers will ensure that the acquired video frame is complete and not corrupted in cases where the image transfer to host system memory may be interrupted and delayed by other host system processes. That is, there is no interruption to the image acquisition of one buffer by any delays in transfer of the other buffer (which contains the previously acquired video frame) to system memory.

- If allocation for the requested number of buffers fails, the driver will reduce the number of on-board frame buffers requested until they can all fit.
- If there is not enough memory for 2 on-board buffers, the driver will reduce the size such that it allocates two partial buffers. This mode is dependent on reading out the image data to the host computer faster than the incoming acquisition.

The maximum number of buffers that can fit in on-board memory can be calculated as follows:

$$\frac{Total\ On - Board\ memory}{Buffer\ Size\ in\ Bytes + 256\ Bytes\ used\ to\ store\ the\ DMA}$$

Dual Camera Input Configuration

When using the dual camera input configuration, the total on-board memory is divided evenly between the 2 inputs.

For example, assuming 512MB of on-board memory and acquiring 1024 x 1024 x 8 bit images, the number of on-board buffers would be:

$$\frac{512\ MB}{(1024\ x\ 1024) + 256} = 511.875\ \geq 511\ on - board\ buffers$$

When running the board in the two Base Camera Link configuration, each input is assigned half of the on-board memory. In the case where there are 512 MB of on-board memory, each input will be assigned 256 MB.

Symptoms: CamExpert Detects no Boards

When starting CamExpert, with no Teledyne DALSA board detected, CamExpert will start in offline mode. There is no error message and CamExpert is functional for creating or modifying a camera configuration file. If CamExpert should have detected an installed board frame grabber, troubleshoot the installation problem as described below.

Troubleshooting Procedure

When CamExpert detects no installed Teledyne DALSA board, there could be a hardware problem, a system bus problem, a kernel driver problem, or a software installation problem.

- Make certain that the card is properly seated in PCIe slot.
- Perform all installation checks described in this section before contacting Technical Support.
- Try the board in a different PCIe slot if available.

Symptoms: Xtium-CL MX4 Does Not Grab

You are able to start Sapera CamExpert but you do not see an image and the frame rate displayed is 0.

- Verify the camera has power.
- Verify the Camera Link cable is connected to the camera.
- Verify the camera and timing parameters with the camera in free run mode.
- Verify you can grab with the camera in free run mode.
- Make certain that you provide an external trigger if the camera configuration file requires one. Use the software trigger feature of CamExpert if you do not have a trigger source.
- Make certain that the camera configuration is the required mode. This must match the camera configuration file. Refer to your camera datasheet.
- Try to snap one frame instead of continuous grab.
- Perform all installation checks described in this section before contacting Technical Support.

Symptoms: Card grabs black

You are able to use Sapera CamExpert, the displayed frame rate is as expected, but the display is always black.

- Set your camera to manual exposure mode and set the exposure to a longer period, plus open the lens iris.
- Try to snap one frame instead of continuous grab.
- Make certain that the input LUT is not programmed to output all '0's.
- A PCIe transfer issue sometimes causes this problem. No PCIe transfer takes place, so the frame rate is above 0 but nevertheless no image is displayed in CamExpert.
- Make certain that BUS MASTER bit in the PCIe configuration space is activated. Look in PCI Diagnostics for **BM** button under "Command" group. Make certain that the **BM** button is activated.

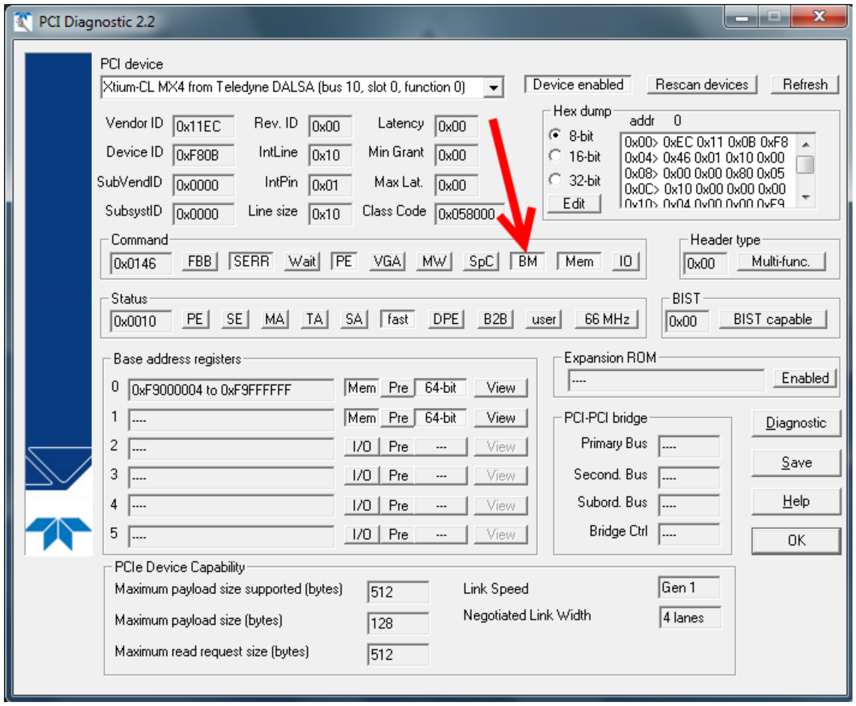


Figure 54: PCI Diagnostic – checking the BUS Master bit

- Perform all installation checks described in this section before contacting Technical Support.

Symptoms: Card acquisition bandwidth is less than expected

The Xtium-CL MX4 acquisition bandwidth is less than expected.

- Review the system for problems or conflicts with other expansion boards or drivers.
- Remove other PCI Express, PCI-32 or PCI-64 boards and check acquisition bandwidth again. Engineering has seen this case where other PCI boards in some systems cause limitations in transfers. Each system, with its combination of system motherboard and PCI boards, will be unique and must be tested for bandwidth limitations affecting the imaging application.
- Is the Xtium-CL MX4 installed in a PCI Express x16 slot?
  Note that some computer's x16 slot may only support non x16 boards at x1 or not at all. Check the computer documentation or test an Xtium-CL MX4 installation. The speed at which the board is running can be viewed using the Diagnostic Tool provided with the driver.
- Is the Xtium-CL MX4 installed in a PCI Express Gen1 slot?
  Some older computers only have PCIe Gen1 slots. Check the status LED to verify if the board is in Gen2 x4 mode; refer to the Status LED Functional Description section. The Generation at which the board is running can be viewed using the Sapera LT PCI Diagnostic or the Diagnostic Tool provided with the driver.

Symptoms: PoCL does not power the camera

If the Xtium-CL MX4 does not power the camera, do the following:

- Ensure that a spare power supply connector from the PC power supply is connected to J7.
- If the camera is powered by means of multiple connectors, make sure all the necessary connections are made between the camera and the frame grabber.
- Ensure that Power-over-CL (PoCL) is enabled. CamExpert can be used to verify that the PoCL parameter, available in the Basic Timing category, is set to Enable.

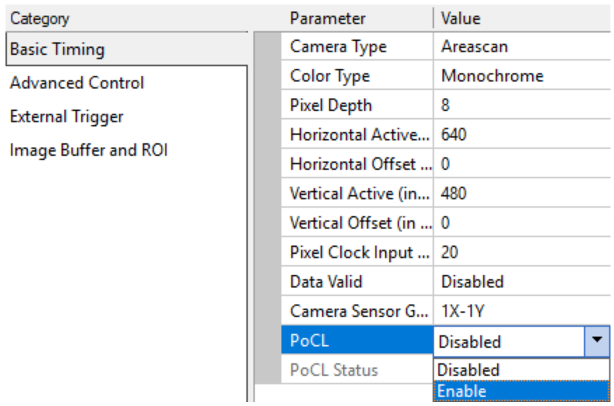


Figure 55: CamExpert PoCL Parameter

- If PoCL is enabled in CamExpert, check that the Video status PoCL of the respective connection is green.

Figure 56: CamExpert Video Status Bar

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Technical Support

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